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Characterization of $Si_{0.25}Ge_{0.75}$-FinFET as a Temperature Nano Sensor

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ABSTRACT This study addresses the impact of thermal sensitivity on the performance of FinFET transistors, with a focus on the role of different channel lengths in enhancing electrical performance. As semiconductor technology advances, understanding the effects of temperature on electronic devices becomes essential to ensure their stability in various applications. Semiconductor manufacturing has stuck to Moore's law, which requires reducing the size of transistors to magnify integration and reduce costs, but biosensors with classic planar transistors are receptive to the effects of short channels, leading to increased power wastage and minimizing sensitivity. FinFET structure shows higher-level gate control, increased repression of short-channel issues. The research uses simulation techniques to study the current-voltage (I-V) behavior in a FinFET structure that relies on $Si_{0.25}Ge_{0.75}$ as the channel semiconductor material. The effect of different temperatures (275, 300, 325, and 350 °K) with channel lengths of 10, 20, and 30 nm is analyzed, focusing on the change in current (ΔI) within the operating voltage range of 0 to 1 V (V_{DD}). The results reveal that thermal sensitivity increases with the reduction of channel length, especially between 10 and 20 nanometers, where the optimal length is found to be 20 nm, due to its balance between low threshold voltage and reduced drain-induced barrier lowering (DIBL), while maintaining stable performance within the studied temperature range. The study also showed that the device operates efficiently at a drain voltage (Vd) of 0.9 volts, ensuring stable performance in the range of 325-350 Kelvin. These results highlight the importance of adjusting design parameters to improve the thermal response of FinFETs, contributing to the development of semiconductors and their applications in nanotechnology and advanced electronics.

INDEX TERMS SiGe-FinFET, temperature, nano-sensor, sensitivity, MOSFET.

I. INTRODUCTION

Early recognition of infection in healthcare can effectively control diseases and reduce medical costs, especially keeping in mind that several diseases lack clear signs through their initial stage. Though biosensors based on field-effect transistors (FETs) are remarkable for label-free sensing ability, miniaturization, and agreement with CMOS technology, the semiconductor manufacturing has stuck to Moore's law, which requires reducing the size of transistors to magnify integration and reduce costs. Even so, when the scale of transistors has been shrunken, biosensors with classic planar transistors are receptive to the effects of short channels, leading to increased power wastage and minimizing sensitivity [1]. Numerous new FET structures, like dual-gate FET [2], FinFET [3], and TFET [4], have been proposed as prospective solutions to this issue. FinFET structure shows higher-level gate control, increased repression of short-channel issues [5], and make better characteristics of biosensors when compared to dual-gate FET.

FinFET technology does, however, provide some optimization issues related to semiconductor manufacturing techniques and theoretical modeling. These constraints so call for further creativity and improvement to raise their efficiency. One of the applications of semiconductors in sensors is temperature sensors [6]. These sensors use nanowire transistors, produced after device current voltage characteristic analysis at various temperatures. This method allows rather high precision of temperature readings [7–10]. Furthermore, employed as diodes are bipolar transistors to provide very accurate temperature monitoring. When employing MOSFETs in temperature sensors, the gate might be connected to either the drain or the source to detect temperature. The capacity of diodes, resistors, capacitors, and transistors to produce extremely compact circuits qualifies them for integration in contemporary electronics and emphasizes the need of developments like FinFET technology in the present-day electronics.

As conventional MOSFETs approach their limitations in terms of practical use, it is essential that field-effect transistor (FET) technology continues to progress. Although MOSFETs have shown innovative ideas in the field of electronics, research on nanoscale FET design is desperately needed to push the boundaries of efficiency and performance. Establishing research, development and manufacturing

techniques that will allow the complete implementation of such future technologies depends on this kind of study. Unlike other FETs, FinFETs have certain advantage over the conventional bulk silicon devices in circuit design [11]. Whereas partly depleted SOI is efficient at temperatures of up to 225 °C, entire depletion of Silicon-On-Insulator (SOI) has been recorded at high temperatures of 275 to 300 °C. By contrast, maximum working temperature of bulk silicon devices is 200°C. Heat resistance of FinFETs makes them perfect for high-performance applications. Moreover, a significant consideration is the reliability of integrated circuits (ICs) under high heat loads, especially for devices like oil drill bit sensors and car systems close to engine blocks. These difficulties highlight the need of ongoing innovation in FET technology for raising the reliability and performance of electronic devices under demanding conditions.

The result of the development of semiconductor technology are FinFETs that surpass the constraints of the conventional planar transistors [12]. Reducing the short-channel effects and manufacturing ultra-small semiconductor devices at the nanoscale depend on these cutting-edge technologies [13-18]. However, there are several downsides to FinFETs, including self-heating, which is a significant drawback despite the many benefits that it provides. The three-dimensional design of the devices may exacerbate this issue, diminishing overall performance. Manufacturers must therefore find out how temperature influences the dependability and effectiveness of the gadget. Moreover, the complexity of the contemporary integrated circuits including a lot of transistors makes modeling of FinFET difficult. The electrothermal modeling must be effective to produce the temperature distribution across the device. This may be accomplished by separating the construction into many sections so that the heat flow and temperature at the surfaces remain constant. In essence, FinFET technology represents a significant development over the classic silicon transistor; yet various issues still need to be resolved to increase the dependability and performance of the device.

FinFET technology is gaining interest because of its promise to increase semiconductor device performance. Little variations in thermal behavior shown by preliminary studies using finite element simulations point to the possibility of great temperature forecast accuracy from these models. Early-stage research has great potential to provide strong models capable of improving the temperature control precision in FinFET devices [19]. During the manufacturing process, the co-fabrication of gate dielectrics is one of the most important benefits of FinFET fabrication. This co-fabrication considerably minimizes the level of contamination that may occur. Moreover, the lithographic exposure and patterning for gate electrodes are done uniformly, thereby reducing gate misalignment. This top-down integration strategy allows for the use of traditional materials instead of standard CMOS, which may result in improved device performance. The manufacturing process does not, however, not without difficulties. Comparatively to conventional Silicon-On-Insulator (SOI) devices, the etching process—which controls the width and thickness of the devices—may cause minor variances. Advancement of FinFET technology and maximum utilization of it in contemporary electronics depend on an awareness of these limitations.

The article focuses on $Si_{0.25}Ge_{0.75}$-FinFET technology and how it might help advance semiconductor devices, particularly when they shrink to the nanoscale scale. Emphasizing the benefits and drawbacks of every device configuration, it addresses numerous ones. Crucially for next electronics applications, the simulations of the study provide interesting insights on how different setups could affect device scalability and performance. To expand the availability of FinFET devices, the paper also suggests strategies to cut the expenses related to their production and installation [20]. The electrical and temperature characteristics of $Si_{0.25}Ge_{0.75}$-FinFET with channel length are also investigated. TABLE 1 presents the advantages of FinFET structure and this study is crucial for the aim of enhancing gadget performance. Physical gates either present or absent, the $Si_{0.25}Ge_{0.75}$-FinFET is categorized as a multi-gate transistor design that enhances channel control and efficiency [21–22]. All things considered, this work provides comprehensive research of FinFET technology stressing its electrical characteristics, economic implications, and combinations, therefore aiding the ongoing development of semiconductor design.

TABLE 1
Advantages of FinFET

Parameters	Details
Power	a) FinFETs have high power efficiency, which allows for better integration. b) In high-performance systems, early adopters reported energy savings of up to 150%.
Operating voltage	a) FinFETs low threshold voltage (VT) allows them to operate well at lower voltage levels. b) This reduces power loss and improves thermal management, making them ideal for portable and energy-intensive applications.
Feature size	a) FinFET technology enables breaching the 20 nm barrier, which was previously thought to be the limit for planar devices. b) - This discovery allows for increased device density and improved performance, hence advancing semiconductor scaling.
Static leakage current	a) Static leakage current is decreased by up to 90%, considerably increasing energy efficiency in idle periods. b) - This is especially helpful for systems that run on batteries, as leakage current is a big issue.
Operating speed	a) FinFET variants are usually 30% quicker than non-FinFET counterparts. b) Faster signal processing is ensured by reduced short-channel effects and enhanced electrostatic control over the channel.

This research aims to study the effect of temperature on FinFET structures that rely on $Si_{0.25}Ge_{0.75}$ as the channel semiconductor material. It primarily focuses on determining the optimal channel length among the available options (10, 20, and 30 nm) to achieve the highest thermal response and improve the overall performance of the device within the operating voltage range of 0 to 1 V (V_{DD}). This study contributes to a deeper understanding of the temperature sensitivity of FinFETs, providing a detailed analysis of the impact of channel length variation on the thermal response of the device, thereby aiding in the interpretation of its operational behavior under different thermal conditions. Among the important findings of the research, it was determined that a channel length of 20 nm provides the optimal balance between performance and thermal response,

making it the best choice when designing future FinFET devices aimed at high-efficiency applications. Additionally, the study relies on advanced simulation techniques to accurately model the current-voltage (I-V) characteristics, which contributes to the improvement of modeling tools used in semiconductor research. The research results also provide clear guidelines on how to adjust the design parameters of these devices to ensure their effective performance in environments with varying temperatures, thereby offering a scientific reference for engineers and researchers working in the field of FinFET and advanced semiconductor technologies.

II. METHODOLOGY

FIGURE 1 presents the explored FinFET structure in this work. The features of the FinFET transistor were evaluated in this work using MuGFET model [23–25]. The output characteristic curves of the transistor were investigated under a wide range of conditions and configurations. Several factors, including as gate length and temperature, were investigated on the nanowire transistor utilizing simulation-derived I-V physical characteristics. For nano-dimensional FETs, Purdue University's MuGFET [26] simulation program was used.

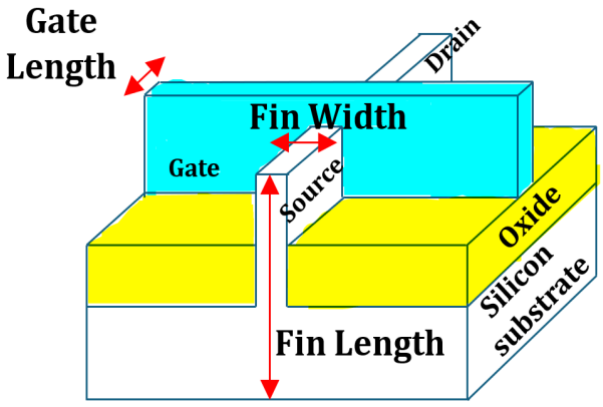

FIGURE 1. FinFET structure.

Bell Laboratories created two potent simulation tools included within MuGFET capabilities: PADRE and PROPHET. While PROPHET is an equation-based solution suited to one, two, or three dimensions [26], PADRE is a flexible device simulator meant for two- or three-dimensional devices with customizable geometries. In the simulation, the P-channel concentration was fixed at cm^{-3}, the channel diameter at 3 nanometers, the source and drain length at 5 nanometers, and the dielectric thickness at 1 nanometer, with tests conducted at 275, 300, 325, and 350 Kelvin.

The Id-Vg relationship in FinFETs was analyzed, focusing on the maximum current change (ΔI) within the operating range of 0-1 volt to evaluate the thermal effect. To ensure the reproducibility of the results, the same standards must be adhered to in order to guarantee consistency in future studies. These programs provide researchers valuable insights by generating normal FET output curves, especially in cases where the physics of FET functioning is adequately stated. Through the use of MuGFET, it is possible to simulate the dynamics of transport by using independent responses to drift-diffusion models [27]. Leading research university in this subject, Purdue University developed and approved the MuGFET nanoHUB. MuGFET tool depends on modeling Nanoscale Multi gate FET architectures (Nanowire and FinFET) with drift-diffusion techniques. Researchers used this technique to reduce losses in nanodevices [28–29] considering the great expense of nanodevices and the large body of research depending on simulation using MuGFET.

In the MuGFET simulation, the following characteristics were employed to replicate the Id-Vg characteristics of FinFETs at various temperatures: channel concentration (P-type), channel width, drain length and source, drain concentration (N-type), and source. Gate width and oxide thickness. FIGURE 2 [30–31] presents an example of the FinFET environment.

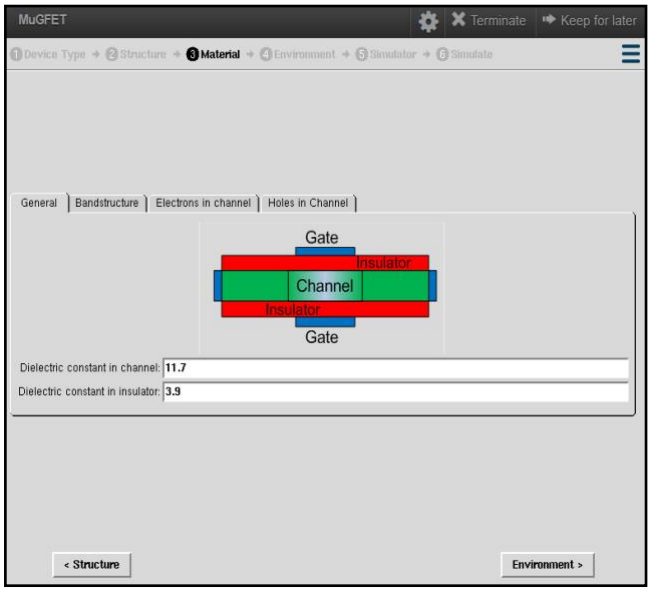

FIGURE 2. Homepage of MuGFET simulation tool.

The I-V characteristics of FinFETs are evaluated using MuGFET, which simulates the electrical behavior based on the user's simulation tool settings. Semiconductor analyzers or SMU units are used in the measurements to measure current and apply voltage, examining both static and dynamic behavior [32] . The devices are calibrated in accordance with established standards to guarantee accuracy. This enables the MuGFET to forecast the device's performance in various scenarios, guaranteeing dependable outcomes.

The Id-Vg characteristics of FinFETs were simulated at temperatures of 275, 300, 325, and 350 K using the following parameters: 5 nm drain and source lengths, equally distributed N-type concentrations, and a 1 nm oxide layer. While the gate doping concentration was fixed at 10^{19} cm^{-3}, the channel diameter was set at 3 nanometers. The maximum current variation (ΔI) defines the FinFET's best temperature sensitivity within the 0–1 V operational voltage range. Moreover, higher oxide thickness results in a drop in drain-induced barrier lowering (DIBL) and a matching change in the threshold voltage. FIGURE 3 shows the electrical activity with respect to width variation.

The thermal sensitivity of FinFET components was evaluated at temperatures of 275, 300, 325, and 350 Kelvin using embedded sensors or calibrated thermocouples for real-time precise measurements. To ensure the accuracy of the results, the sensors were calibrated using standard references, and the temperature was adjusted in an environmental chamber to minimize fluctuations and ensure repeatability. To enhance the reliability of the measurements, precise calibration techniques, thermal control, and repeated measurements were adopted, with results compared to previous studies. This approach contributes to providing

accurate data to understand the impact of heat on the performance of FinFETs under different operating conditions. FIGURE 4 describes the flowchart of methodology of this work.

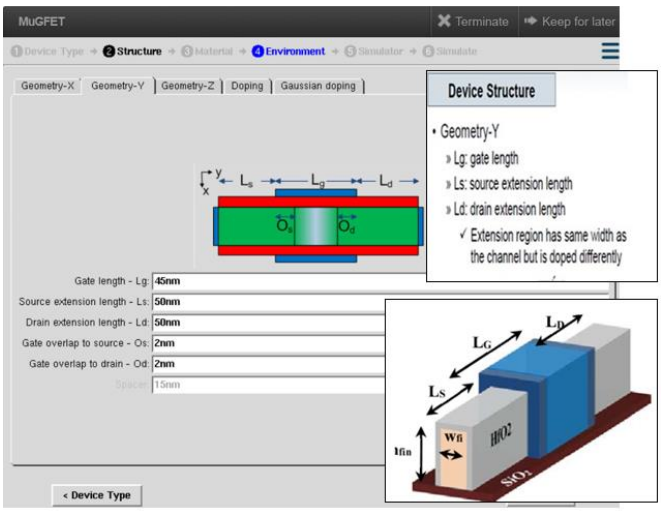

FIGURE 3. **Selection of channel length.**

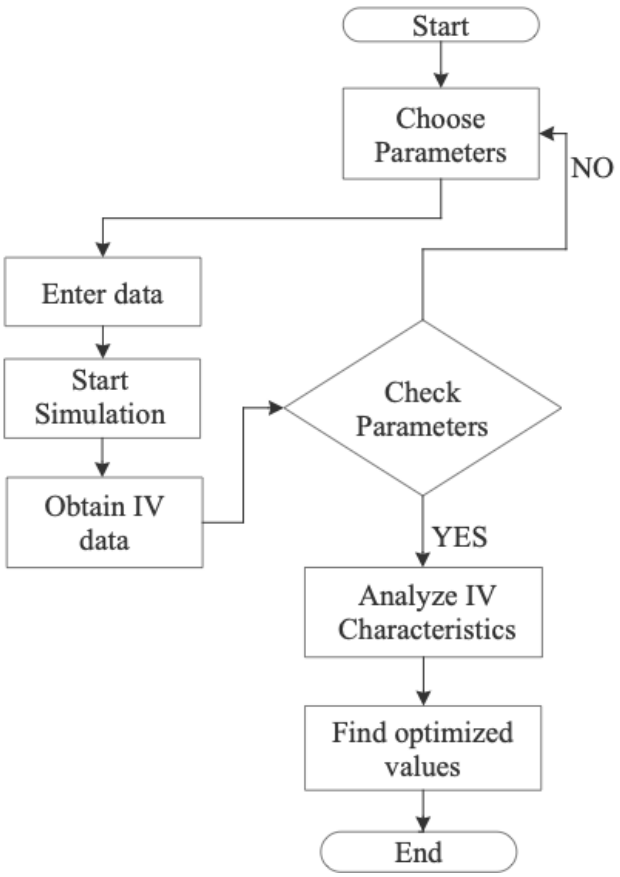

FIGURE 4. **Methodology flowchart of research.**

III. RESULT

FIGURES 5, FIGURES 6, and FIGURES 7 demonstrate with voltage increases of 0.1 V the variation in current (I) resulting from gate lengths (Lg) of 10, 20, and 30 nm. Results show a linear decrease in V_{DD} with an increasing temperature inside the V_{DD} range of 0 to 1 V; lower temperatures show the most sensitivity (max ΔI). At V_{DD} = 0.7 and 0.9 V, the highest temperature sensitivity coefficients are shown in FIGURES 5 and FIGURES 6 for Lg values of 10 nm and 20 nm, respectively. FIGURE 7 displays the highest sensitivity at Lg = 30 nm for V_{DD} = 1 V. These results show that the transistor runs most optimally at a drain voltage (Vd) of 0.9 V, which offers stability over the 325–350 K temperature range as shown in FIGURES 5, FIGURES 6, and FIGURES 7.

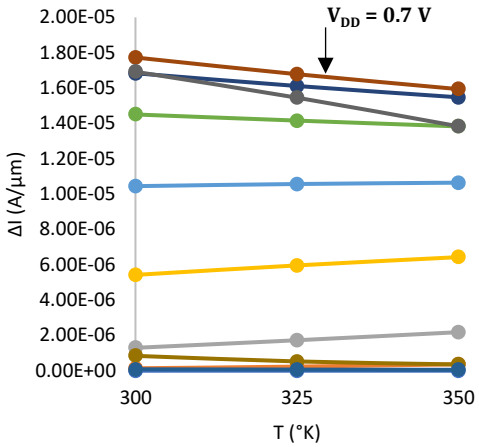

FIGURE 5. **ΔI–T characteristics of FinFET (Wg=10nm, Lg = 10nm).**

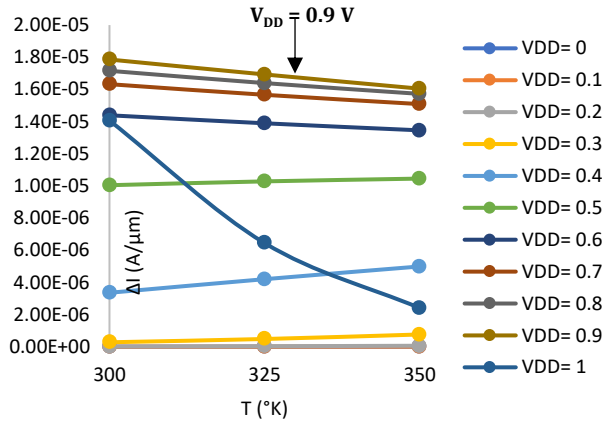

FIGURE 6. **ΔI–T FinFET characteristics (Wg =10nm, Lg=20nm).**

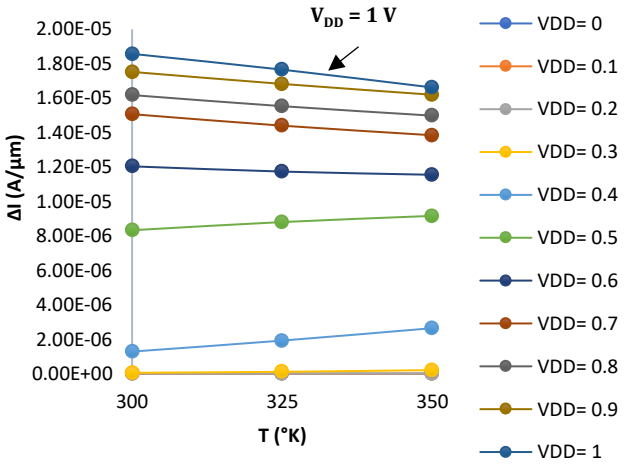

FIGURE 7. **ΔI–T FinFET characteristics (Wg =10nm, Lg=30nm).**

At temperatures of 275, 300, 325, and 350 K, the variations in ΔI that occur as a result of decreasing V_{DD} are depicted in FIGURES 8, 9, and 10. These variations are observed for gate lengths of 10, 20, and 30 nm. V_{DD} values of 0.9 V (Lg = 10 nm), 0.9 V (Lg = 20 nm), and 1 V (Lg = 30 nm) produced maximum sensitivity, or max ΔI. With the ideal voltage at 0.9 V for Lg = 10, 20 nm and Wg = 10 nm, the

outcomes show that ΔI rises with increasing temperature and V_{DD}.

FIGURE 11 depicts the relationship between channel length and optimal temperature sensitivity (max ΔI), as well as the ideal operating voltage (V_{DD}) associated with the highest thermal sensitivity shown in FIGURES 8, 9, and 10. Despite a little change in channel length from 10 nm to 30 nm, the temperature sensitivity jumped significantly up to Lg = 20 nm. After this, the relationship between temperature sensitivity and channel length displayed a linear decrease.

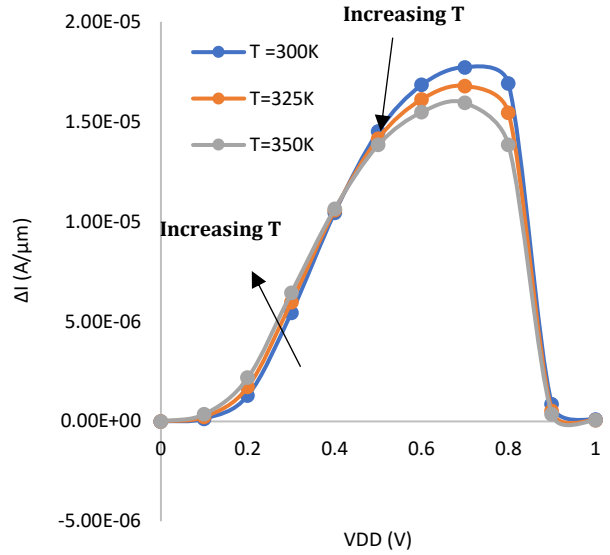

FIGURE 8. FinFET characteristics (Wg=10nm, Lg = 10nm) ΔI–V_{DD}).

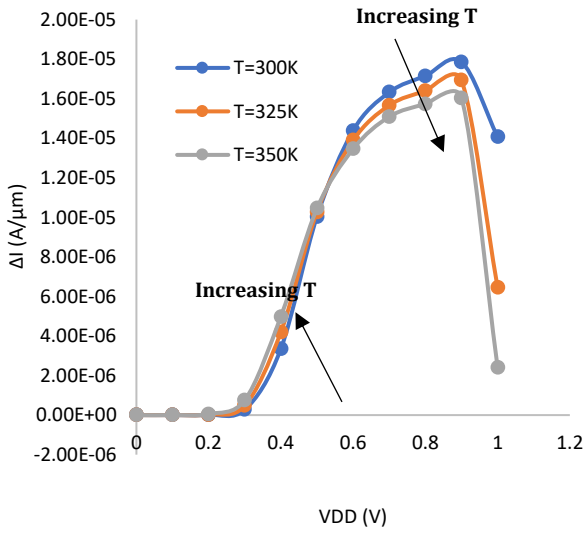

FIGURE 9. FinFET characteristics (Wg = 10 nm, Lg = 20 nm) ΔI–V_{DD}).

FIGURE 12 depicts temperature profiles for important FinFET characteristics such as subthreshold swing (SS), threshold voltage (V_T), and drain-induced barrier lowering (DIBL) evaluated at 275, 300, 325, and 350 K with Lg = 10 nm and Wg = 10 nm. Rising temperature caused V_T to show a linear drop; from 0.33 V at 275 K to 0.27 V at 350 K. As the potential barrier of the channel at the source is reduced, DIBL increases the drain voltage (V_{DD}) and the leakage current in the OFF state, resulting in a decrease in V_T. The ideal SS of 69.5 mV/dec was broken most at 350 K, where SS rose to 172.1 mV/dec from the lowest temperature of 275 K, where it was measured at 231.2 mV/dec. On the other hand, at 350 K, the SS value approaches the ideal of 54.6 mV/dec. DIBL also displayed exponential rise as the temperature climbed. DIBL lowers from 231.17 to 208.29 mV/V. This study finds the best transistor size at Lg = 10 nm and 20 nm at 350 K. V_T grew hyperbolically as oxide thickness rose; DIBL surged exponentially; SS changed linearly. FIGURE 13 depicts the V_T, SS, and DIBL behaviors of the FinFET at 275, 300, 325, and 350 K, with a gate length (Lg) of 20 nm and a width (Wg) of 10 nm. The graph shows that these criteria linearly drop as the temperature rises from 275 to 350 K.

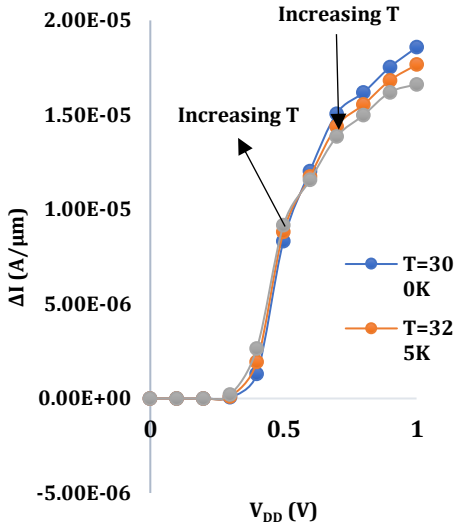

FIGURE 10. FinFET characteristics (Wg = 10 nm, Lg = 30 nm) ΔI–V_{DD}).

Particularly the ranges for SS, DIBL, and V_T are 0.49 to 0.46 V, 32.89 to 45.35 mV/V, and 94.73 to 122.16 mV/dec respectively. At 350 K, the SS value is greater than 94.73 mV/dec, which is the greatest deviation from the ideal SS value of 54.6 mV/dec of the system. The temperature-dependent SS, which rises to 122.16 mV/dec as the temperature rises, is a reflection of the distance from the ideal SS due to the fact that it increases. DIBL also exhibits a higher inclination in connection with temperature.

FIGURE 14 shows further the link between V_T, DIBL, and SS changes and their combined effects on the FinFET's performance at temperatures between 275 and 350 K using Lg = 30 nm and Wg = 10 nm. V_T decreases linearly as temperature increases, with values ranging from 0.58 V at 275 K to 0.549 V at 350 K. DIBL rises from 5.56 to 9.82 mV/V and SS rises from 75.44 to 97.42 mV/dec. The 75.44 mV/dec SS value at 350 K most nearly matches the ideal SS of 54.6 mV/dec. In order to estimate the ideal combination of length and temperature, the electrical properties of the device are utilized. At a temperature of 350 K, the SS increases even further to 97.42 mV/dec, and the DIBL continues to increase with temperature, demonstrating the influence of these properties.

FIGURE 15 depicts the behavior of V_T, DIBL, and SS for different FinFET channel lengths (10-30 nm and Wg = 10 nm). Whereas V_T rises until it approaches saturation beyond a channel length of 20 nm, DIBL drastically drops close to 20 nm at 300 K then gradually increases again. SS drops and approaches the optimal value at 20 nm, suggesting that under the tested conditions this is the ideal
channel length for FinFETs. A channel length of 10 to 30 nm is ideal, as shown in the figure, because SS increases with

temperature while V_T and DIBL decrease. These results confirm earlier studies [33–37] by proving that the electrical properties of FinFETs are linearly correlated with their channel diameters, which span 10 to 30 nm.

Temperature is identified as the most important factor influencing current in FinFETs, owing to the higher carrier velocity observed in n-type FinFETs as fin diameters decrease. Fascinatingly, channel cross-section scaling has hardly effect on carrier velocities in n-type FinFETs. In MOSFETs that have been aggressively downscaled, the effective carrier injection velocity (Vinj) is the factor that determines the drain saturation current that flows from the source to the channel. This carrier injection velocity, a material characteristic independent of mobility, mostly determines the driving current during ballistic transport [38].

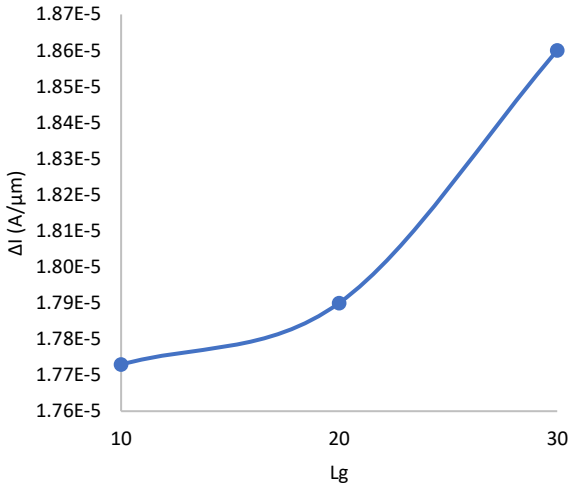

FIGURE 11. Based on the highest temperature sensitivity, the operating voltage V_{DD} was optimized using a range of channel lengths).

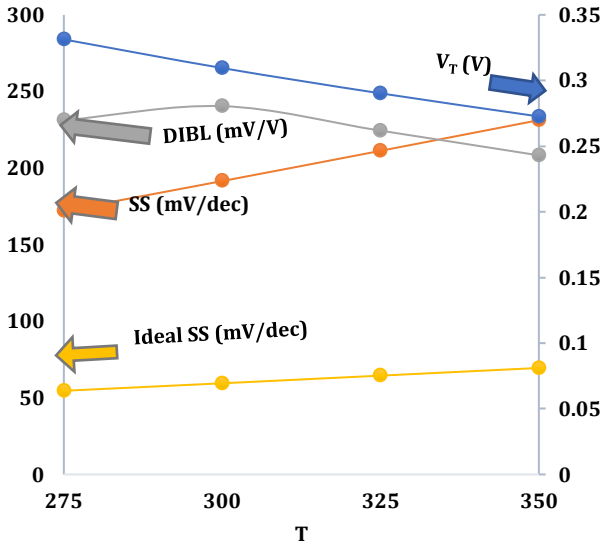

FIGURE 12. V_T, SS and DIBL at Wg=10nm, Lg = 10 nm.).

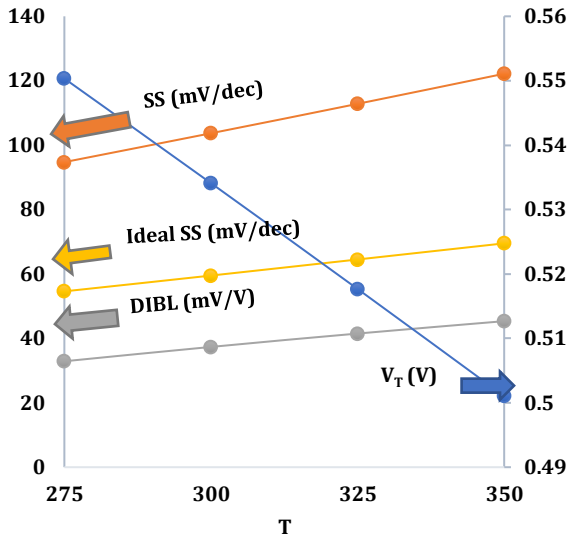

FIGURE 13. V_T, SS and DIBL at Wg =10nm, Lg = 20 nm.).

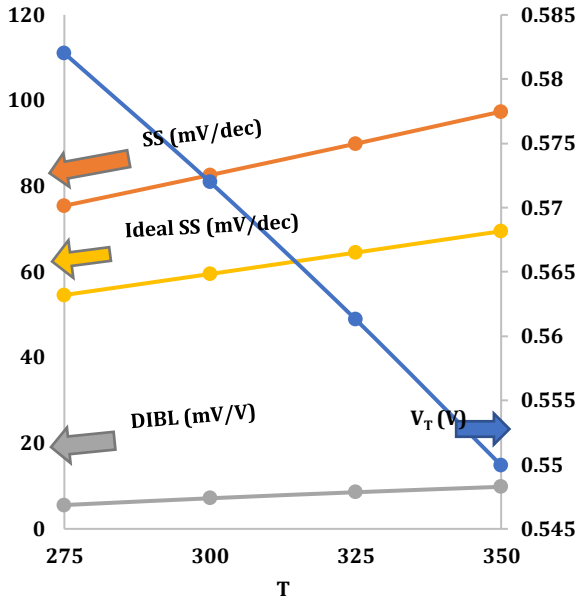

FIGURE 14. V_T, SS and DIBL at Wg =10nm, Lg = 30 nm.).

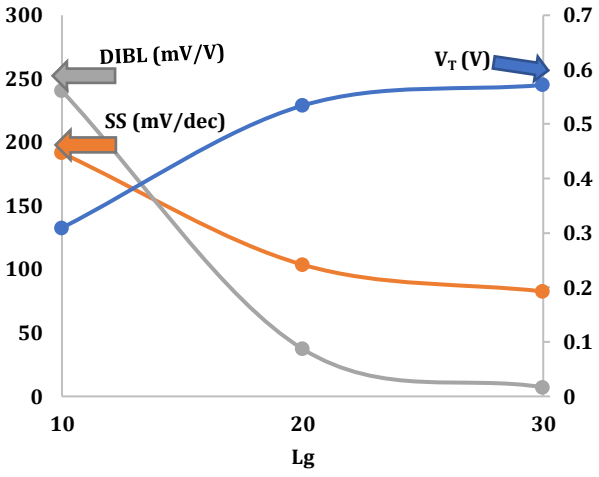

FIGURE 15. V_T, SS and DIBL with Lg.

IV. DISCUSSION

Based on the obtained results, the best performance in reducing SS and DIBL is observed at channel lengths of approximately 20 nanometers. As the channel length exceeds 20 nanometers, both SS and DIBL begin to deteriorate, supporting the notion that a channel length of 20 nanometers offers the optimal balance between electrical performance. These findings are consistent with previous studies that have shown that the electrical characteristics of FinFETs are linearly related to channel lengths in the range of 10 to 30 nanometers, reinforcing those 20 nanometers is the ideal length to achieve the best performance with minimal DIBL and maximum V_T value.

Additionally, the results confirm the increase in thermal sensitivity as the channel length is reduced from 10 to 20 nanometers, emphasizing the importance of controlling temperature effects to enhance device performance. Therefore, 20 nanometers can be considered the optimal channel length for improving the electrical properties of FinFETs. The study results, as shown in TABLE 2, demonstrate that thermal sensitivity increases with the reduction of channel length from 10 to 20 nanometers, with 20 nanometers identified as the optimal length, which contrasts with studies focusing on longer channel lengths. Key performance indicators for FinFET devices with different gate lengths are shown in this table. As the gate length grows, the subthreshold swing and drain-induced barrier lowering values improve, suggesting improved control of the short-channel effect. As anticipated given the increasing gate control over the channel, the threshold voltage likewise rises with gate length.

The findings of this study on FinFET transistors are displayed in TABLE 2, which demonstrates how the short-channel effects (SS, DIBL, and V_T) change with varying gate lengths (Lg) while maintaining a fixed gate width (Wg) of 10 nm. This table shows that as Lg increases, the Subthreshold Slope (SS) improves (decreases), indicating improved switching behavior for longer gate lengths. As Lg increases, DIBL significantly decreases, indicating improved electrostatic regulation and less short-channel effects. As Lg rises, the threshold voltage (V_T) rises marginally, as would be predicted given the decrease in short-channel effects.

The voltage shift needed to increase the drain current by a factor of 10 in the subthreshold zone of operation is represented by the SS values (subthreshold swing) in the table that is provided. Sharper switching characteristics and improved gate control over the channel are indicated by a lower SS value.

SS = 166.8 mV/dec in this table and at Lg = 10. Because short-channel effects are more noticeable at shorter gate lengths, this comparatively high number indicates less effective gate control. However, SS = 93.65 mV/dec at Lg = 20. Better gate control as the gate length grows is indicated by this notable improvement over Lg = 10. whereas SS = 75.44 mV/dec at Lg = 30. Out of all the given gate lengths, the one with the lowest SS value indicates the most effective gate control. This improvement is anticipated as gate length increases and short-channel effects become less significant. Similar SS values for a FinFET device are displayed in [39], which also notes reaching a peak value of 72.43 mV/dec. This supports the pattern seen in this table, which shows that the subthreshold swing improves with increasing gate length. Longer gate lengths typically result in a lower subthreshold swing, which in turn reduces leakage current and boosts power efficiency in FinFET devices.

TABLE 2 offer important insights into the performance traits of FinFET devices. As the gate length rises, the SS and DIBL values fall while the V_T increases, according to this table, which displays the subthreshold swing, drain-induced barrier lowering, and threshold voltage for various gate lengths.

The results presented in TABLE 2, which showed that FinFET devices have higher performance and scalability down to the 10 nm regime, are in line with this trend. The gate-all-around architecture's improved gate control is responsible for the observed gains in SS and DIBL. The results showed that the 20-nanometer channel achieves the optimal balance between thermal sensitivity and electrical performance, as this length contributes to reducing the threshold voltage (V_T) and minimizing the drain-induced barrier lowering (DIBL) phenomenon, along with improving the subthreshold slope (SS), thereby enhancing the efficiency of FinFET devices. In the future, it will be necessary to improve simulation models to explore the effects of temperature in more detail, in addition to testing new semiconductor materials and studying their stability under long-term operating conditions to enhance device reliability.

This study highlights the improvements in electrical properties at this optimal channel length and enhances the accuracy of the results through MuGFET simulations, contributing to the advancement of semiconductor technologies. Furthermore, the study provides valuable guidelines on how temperature and channel length influence the electrical performance of devices, offering a deeper understanding of how these factors affect device characteristics. In conclusion, TABLE 3 summarizes the comprehensive findings of this study, confirming that 20 nanometers is the ideal channel length for performance optimization.

With the reported SS and DIBL values ranking among the best among the cited research works [37]-[39], the comparison table (TABLE 3) further emphasizes the competitiveness of the current study. TABLE 3 compares the best SS and DIBL values from different research studies. SS in present study achieves 75.44 mV/dec, which is competitive with other studies. DIBL in this study reports a DIBL of 5.56 mV/V, which is significantly lower than most prior studies, indicating better electrostatic control.

TABLE 3 related with comparison with another research works, showcases the achieved subthreshold swing and drain-induced barrier lowering values of your work against other research. A lower SS value indicates better gate control and sharper switching, while a lower DIBL value signifies reduced short-channel effects. This study's best SS (75.44 mV/dec) is comparable to other reported best values (60-80 mV/dec). However, your DIBL (5.56 mV/V) is significantly lower, showcasing substantially improved short-channel effect suppression compared to other works (10-139.52 mV/V). This highlights the potential advantages of your FinFET design in achieving both good performance and reduced short-channel effects. The SS value in this research is competitive, the increasing V_T trend with Lg aligns with expectations and suggests that FinFET scaling impacts threshold voltage control.

TABLE 2
Our research results

Wg = 10 (nm)	SS (mV/dec)	DIBL (mV/V)	V_T (V)
Lg = 10	166.8	191.19	0.37
Lg= 20	93.65	25.1	0.56
Lg = 30	75.44	4.11	0.58

TABLE 3
Comparison with another research works

Reference	Best value of SS	Best value of DIBL
[37]	72.43 mV/dec	139.52 mV/V
[38]	80 mV/dec	10 mV/V
[39]	73 mV/dec	28mV/V
[40]	63 mV/dec	10 mV/V
Present study	75.44 mV/dec	5.56 mV/V

V. CONCLUSION

This research aimed to study the effect of temperature on FinFET structures that use $Si_{0.25}Ge_{0.75}$ as the channel semiconductor material, focusing on how different channel lengths (10, 20, and 30 nanometers) affect electrical performance under various thermal conditions. The results showed that the 20-nanometer channel achieves the optimal balance between thermal sensitivity and electrical performance, as this length contributes to reducing the threshold voltage (V_T) and minimizing the drain-induced barrier lowering (DIBL) phenomenon, along with improving the subthreshold slope (SS), thereby enhancing the efficiency of FinFET devices. The study also highlighted the significant impact of temperature, especially at channel lengths between 10 and 20 nanometers, where thermal variations become more pronounced, making it crucial to adjust device design according to thermal conditions in semiconductor development. In the future, it will be necessary to improve simulation models to explore the effects of temperature in more detail, in addition to testing new semiconductor materials and studying their stability under long-term operating conditions to enhance device reliability. In addition, the combination of FinFET technology and recent advancements in quantum computing may open new horizons in the field of advanced electronics, contributing to significant leaps in nanotechnology and improving the efficiency of future electronic devices.

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