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Power Added Efficiency Enhancement in a 2.4 GHz Class E Power Amplifier in 0.13µm CMOS Technology

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ABSTRACT Power-Added-Efficiency (PAE) is one of the most significant factors by which the performance of a Power Amplifier (PA) can be scrutinized. A new approach to increase PAE is proposed in this paper. Plus, the trade-off between increasing VDD for more output power and more PAE is examined. In addition, new and precise calculations for both output voltage and output power are achieved. Furthermore, the concept of using an equivalent circuit of a transformer is described to justify the new way to increase PAE. The designed Power Amplifier (PA) operates at 2.4GHz. The simulation is performed by Advanced Design System (ADS) and MATLAB. Plus, the TSMC 0.13 µm CMOS process is utilized to fulfil the procedure. The class E PA is designed to gain two different objectives, including more output power and more PAE. With VDD= 1.18 V the output power is 19.52 dBm and PAE is 68.5 %. Ultimately, with VDD=4.4 V the output power is 31.24 dBm and PAE is 62.7 %.

INDEX TERMS Power Amplifier, Class E, PAE Enhancement, CMOS.

I. INTRODUCTION

A Power amplifier is an integral part of radio frequency transmitters. Major criteria, consisting of output power, Power-Added-Efficiency (PAE), and linearity, have been considered to evaluate the performance of power amplifiers. In fact, the higher the output power and PAE are, the better a PA will be. The main duty of a PA is to strengthen the power of the input signal. Generally, power amplifiers can be categorized in two different classifications according to the role of the CMOS transistor. If the CMOS plays as a current source, the PA is class A, B, AB, or C. Plus, the PA is class D, E, or F provided that the CMOS acts as a switch. In addition, power amplifiers can be considered as either linear, Classes A, B, and AB, or non-linear, including classes C, D, E, and F [1]. It has been proven that a class-A amplifier has less efficiency than a class B amplifier [2, 3]. To enhance the efficiency, the combination of both class-A and class-B, called class-AB, is utilized [1]. Class-C, however, have more distortion, noise effects, and efficiency [4]. In addition, class-E has better power efficiency than class-D and class-F [1, 5, and 6].

Briefly, various architecture of PA has been proposed with different objectives. Cascode modulated CMOS PA, parallel class-AB, and two-stage class-E have used cascode topology to create a PA [7-11]. Moreover, Self-Biased technique is used to reduce the power consumption of the circuit [12]. The area of the circuit implementation is decreased and the reverse isolation is enhanced by using capacitive cross coupling technique [13]. The differential cascode PA is designed to reduce the common mode noise and the time delay [14-16]. Furthermore, the capacitive cross-coupling neutralization technique is utilized to decline the inductor loss in a PA [17-19]. Ultimately, to increase the output power of a PA, the power combining technique is used [20, 21].

In this paper, the new calculation and formulae relating to output power and output voltage of the PA are calculated. Plus, a new topology is proposed to increase the PAE of the PA. Furthermore, the performance of the circuit in 0.13 µm CMOS technology with different voltage supplies is evaluated and compared.

II. THE EQUIVALENT AND CONCEPT OF TRANSFORMERS

Generally, a transformer consists of primary and secondary windings, demonstrated in figure 1. The important formulae clarifying the performance of a transformer are mentioned from equation (1) to equation (3). The main concept of transformers is that transformers can either amplify or attenuate the voltage applied to the primary terminal in accordance with their Winding ratio. In fact, if the number of turns of the secondary winding (N2) is bigger than the number of turns of the primary winding (N1), the voltage in the secondary terminal (V2) is amplified. Plus, if N2 is smaller than N1, the voltage is attenuated. In addition, the impedance seen from the primary terminal (ZIN) can either diminish the impedance existing in the secondary terminal (ZOUT) or increase ZOUT according to the Winding ratio. Thus, a transformer can be utilized for voltage amplification, voltage attenuation, and impedance matching.

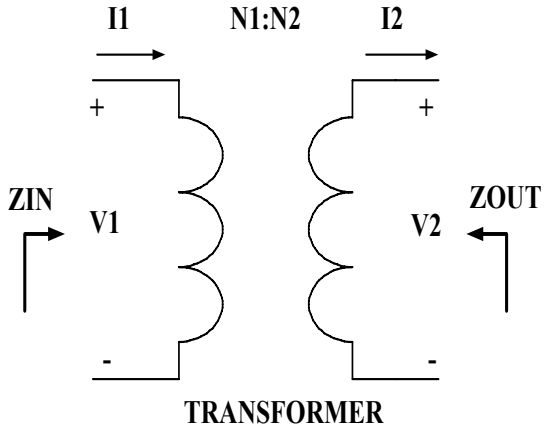

FIGURE 1. The Ideal transformer

$$V1 = (\frac{N1}{N2}) \times V2 \quad (1)$$

$$I1 = (\frac{N2}{N1}) \times I2 \quad (2)$$

$$ZIN = (\frac{N1}{N2})^2 \times ZOUT \quad (3)$$

In which:
V1: Primary voltage.
V2: Secondary voltage.
I1: Current flowing into the primary terminal.
I2: Current flowing out of the secondary terminal.

$N = (\frac{N2}{N1})$: Winding ratio.

However, when it comes to the performance of the circuit in high frequencies and integrated circuits, transformers are very big and are not appropriate for high frequencies. Furthermore, they can not be designed to operate at a specific frequency. To resolve the problem, an equivalent circuit of transformers should be used, illustrated in figure 2. Indeed, the major objective of the equivalent circuit is that the input voltage (VIN) should be amplified at a particular frequency. The relationship between the output voltage (VOUT) and the input voltage (VIN) is given in equation (4) and equation (5).

$$VOUT = N \times VIN \quad (4)$$

In which:

$$N = \frac{(C1 \times L1 \times ZL \times S^2)}{(ZL + (L1 + L2) \times S + C1 \times ZL \times L1 \times S^2 + C1 \times L1 \times L2 \times S^3)} \quad (5)$$

$$S = 2 \times \pi \times f \times j \quad (6)$$

$$j = \sqrt{-1} \quad (7)$$

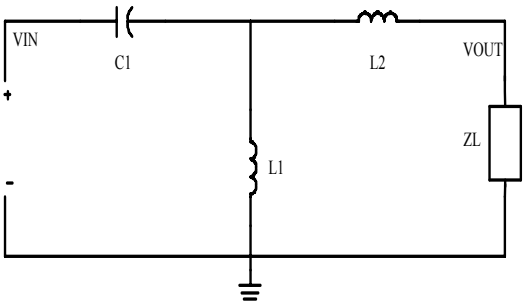

FIGURE 2. The Equivalent circuit of the transformer

Therefore, the equivalent circuit works like a transformer with the Winding ratio (N). The advantages of using the equivalent circuit over a real transformer can be specified as:

1- Owing to Complementary metal–oxide–semiconductor (CMOS) technology, all elements existing in the equivalent circuit can be built in a very small area.
2- By calculating the value of the elements appropriately, the circuit can perform properly at the desired frequency.
3- Unlike the Winding ratio of a real transformer which is a real number, the Winding ratio of the equivalent circuit can be either a real number or a complex number.

To justify the utilization of a transformer in a Power Amplifier (PA), the formula of Power-Added-Efficiency (PAE) in equation (8) should be scrutinized.

$$PAE = \frac{P_{OUT} - P_{in}}{P_{DC\,total}} \quad (8)$$

In order to increase PAE, three approaches might be considered:

1- Increasing the output power (P_{OUT}).

2- Decreasing the input power (P_{in}).
3- Decreasing the power consumed with the DC voltage supply ($P_{DC\,total}$).

The main focus is given into decreasing the input power. The input power can considerably decline if the voltage applied to the input of the PA is reduced. To facilitate the circumstance, the input voltage should be amplified prior to being applied to the input. Therefore, an equivalent circuit of a transformer is utilized at the input of the PA, located between the input voltage supply and the CMOS switch.

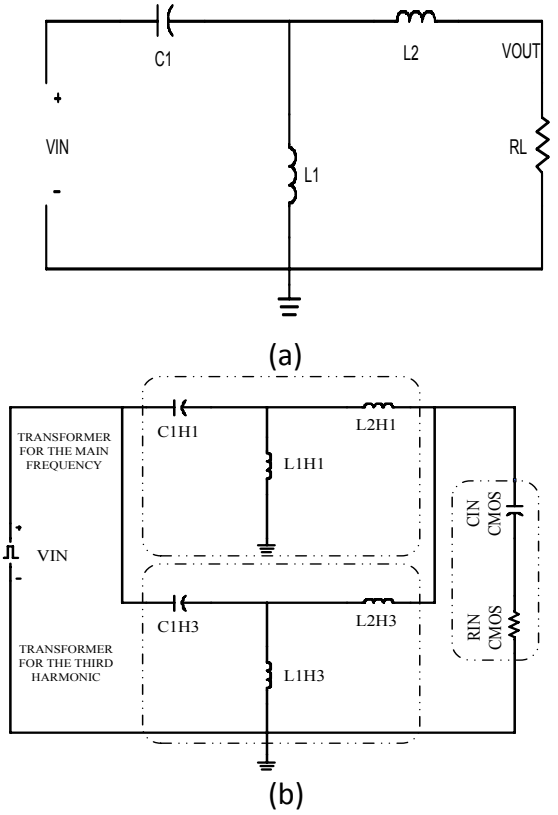

FIGURE 3. (a): The equivalent circuit utilized in the output of the PA. (b): The equivalent circuit utilized in the input of the PA

The equivalent circuit, depicted in figure 3, is used to fulfil three main objectives:

1- At the input of the PA, the transformer should amplify the voltage with the main frequency at which the circuit is supposed to operate.
2- The third harmonic should be added to the input signal to form an appropriate signal for the CMOS switch.
3- The output voltage of the switch should be amplified before being given to the output load (RL).

III. FOURIER SERIES AND THE UTILIZATION OF THE EQUIVALENT CIRCUIT

The input voltage in class E power amplifiers is a pulse. Practically, a pulse has both rise time (tr) and fall time (tf), shown in figure 4. It is assumed that the rise time and the fall time of the pulse are equal (tr=tf). The feature of the pulse can be seen in equation (9).

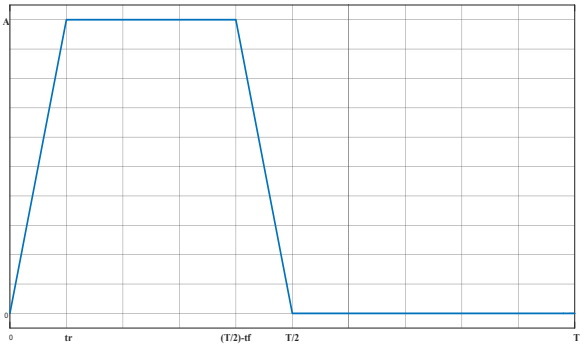

FIGURE 4. The practical pulse with rise time and fall time.

$$x(t)=\begin{cases}\dfrac{A}{tr}\times t & 0<t<tr\\ A & tr<t<\dfrac{T}{2}-tf\\ \dfrac{-A}{tr}\times t & \dfrac{T}{2}-tf<t<\dfrac{T}{2}\\ 0 & \dfrac{T}{2}<t<T\end{cases} \tag{9}$$

The calculation of Fourier series of the pulse is brought from the equation (10) to equation (18).

$$x(t)=a_0+\sum_{n=1}^{\infty}a_n\cos(2\times\pi\times f\times t\times n)+\sum_{n=1}^{\infty}b_n\sin(2\times\pi\times f\times t\times n) \tag{10}$$

$$a_0=\frac{1}{T}\int_0^T x(t)\ dt \tag{11}$$

$$a_n=\frac{2}{T}\int_0^T x(t)\times\cos(\frac{2\times\pi\times t\times n}{T})\ dt \tag{12}$$

$$b_n=\frac{2}{T}\int_0^T x(t)\times\sin(\frac{2\times\pi\times t\times n}{T})\ dt \tag{13}$$

$$a_0=\frac{\mathrm{T}}{8}-\frac{\mathrm{tr}}{2}+\frac{(\mathrm{A}\times\mathrm{tr})}{\mathrm{T}} \tag{14}$$

$$a_n=-\frac{A\times T\times(\cos(\pi\times n)-\cos(\frac{2\times\pi\times n\times tr}{T})-\cos(\frac{\pi\times n\times(T-2\times tr)}{T})+1)}{(2\times\pi^2\times n^2\times tr)} \tag{15}$$

$$b_n = \frac{A \times T \times \left(\sin\left(\frac{2 \times \pi \times n \times tr}{T}\right) - \sin(\pi \times n) + \sin\left(\frac{\pi \times n \times (T - 2 \times tr)}{T}\right)\right)}{(2 \times \pi^2 \times n^2 \times tr)} \quad (16)$$

$$a_n = \begin{cases} 0 & , \quad n \quad odd \\ \dfrac{-A \times T}{n^2 \times \pi^2 \times tr} & , \quad n \quad even \end{cases} \quad (17)$$

$$b_n = \frac{A \times T \times sin\left(\frac{2 \times \pi \times n \times tr}{T}\right)}{(\pi^2 \times n^2 \times tr)} \quad (18)$$

Unlike an ideal pulse with $b_n = 0$ and without any rise time and fall time, the real pulse produces both a_n and b_n, meaning both sine parts and cosine parts in all harmonics should be taken into account. The pulse is comprised of the signal with the main frequency and its harmonics. The third harmonic can play a significant role to create a signal with different ripple. Should the third harmonic is retained approximately constant and the main frequency is amplified, the ripple varies noticeably, demonstrated in figure 5. As an example, the amplitude of the main signal at the main frequency is 0.6366 and it is amplified from 0.6366 V to 3.183 V. The best shape occurs when the main signal at the main frequency is amplified three times (1.9098 V) and the third harmonic is amplified at the low level.

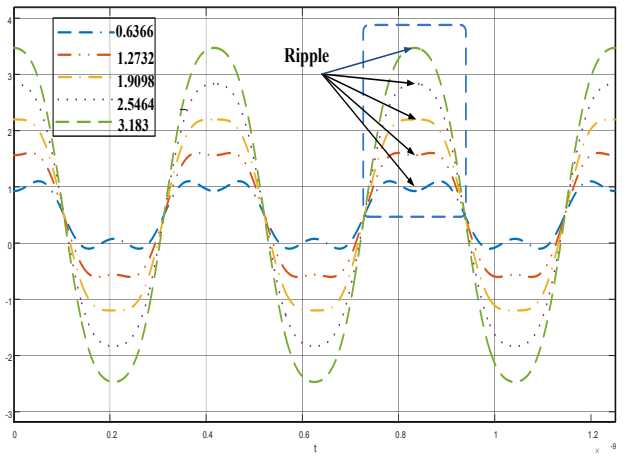

FIGURE 5. The Effect of Amplifying the Main Frequency and The Third Harmonicon on the Ripple

In order to execute the desired pulse, two transformers are required. Indeed, one transformer is used to amplify the signal with the main frequency and the second transformer is utilized to amplify the third harmonic, demonstrated in Figure 6.

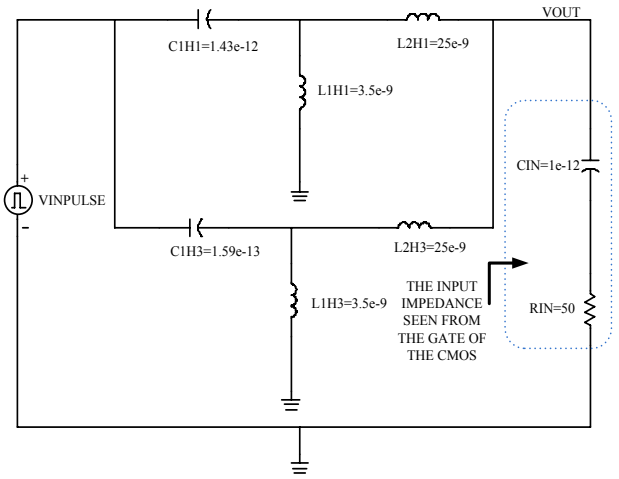

FIGURE 6. The Sample of Using Two Equivalent Transformers.

What is seen at the input of a CMOS is a capacitor and a resistor in series. The capacitor and the resistor are created by capacitors and resistors produced by CMOS in gate, source, and drain. It is crucially significant that the value of the elements existing in the circuit should be calculated within two steps:

1-C1H1, L1H1, and L2H1 are calculated for the main frequency (at 2.4 GHz) and the impedance seen in VOUT is considered at the same frequency, which is ZL (W).

2-C1H3, L1H3, and L2H3 are calculated for the third harmonic (at 7.2 GHz) and the impedance seen in VOUT is considered at the same frequency, which is ZL (3W).

For instance, if the input impedance is a one Pico farad capacitor (CIN=1e-12) in series with a fifty ohm resistor (RIN=50Ω) at the main frequency (f= 2.4 GHz), ZL (W) and ZL (3W) are:

$$ZL(W) = 50\text{-}66.3146 \times \mathrm{j}$$

$$ZL(3W) = 50\ \text{-}22.1049 \times \mathrm{j}$$

Hence, by considering L1H1= L1H3 and L2H1= L2H3, the values of C1H1 and C1H3 can be calculated via equation (4) and equation (5) by substituting ZL with ZL(W) and ZL(3W). In fact, the assumption of L1H1= L1H3 and L2H1= L2H3 can facilitate the circuit implementation because similar components can be built more straightforwardly. The input voltage is a one volt pulse, shown in figure7 (a), and the output voltage (VOUT) is depicted in figure 7(b) and 7(c).

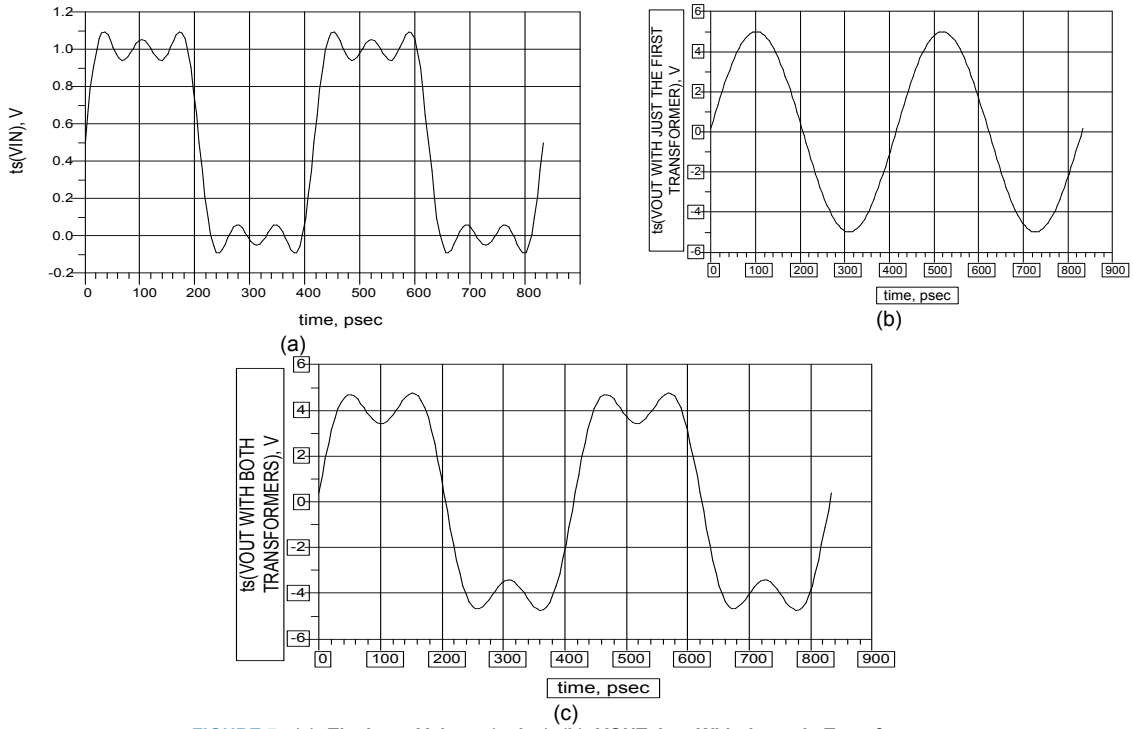

FIGURE 7. **(a): The Input Voltage (pulse), (b): VOUT Just With the main Transformer, (c): VOUT With Both Transformers**

By utilizing just one transformer for the main frequency, the signal is amplified but it is a sinusoidal wave, shown in figure7 (b). To have an amplified pulse, the third harmonic has to be added to the sinusoidal wave via the second transformer to form a pulse, demonstrated in figure7 (c).

The behavior of the transformers at the input of a CMOS is shown in figure 8. Two impedances, ZL (W) and ZL (3W), are considered to calculate the elements in both transformers.

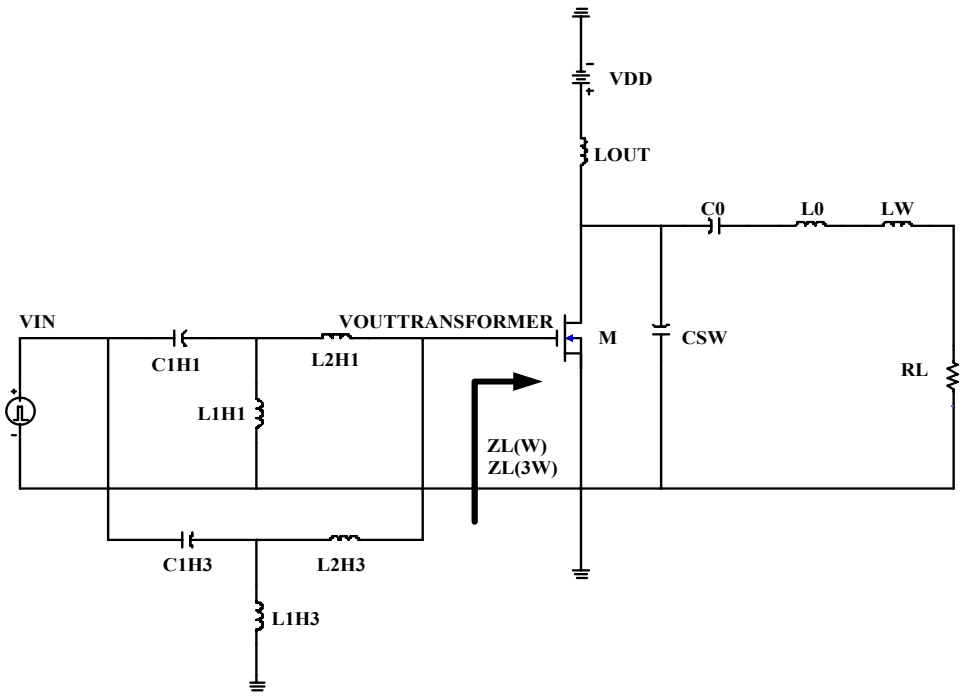

FIGURE 8. **Transformers In The Input of a CMOS**

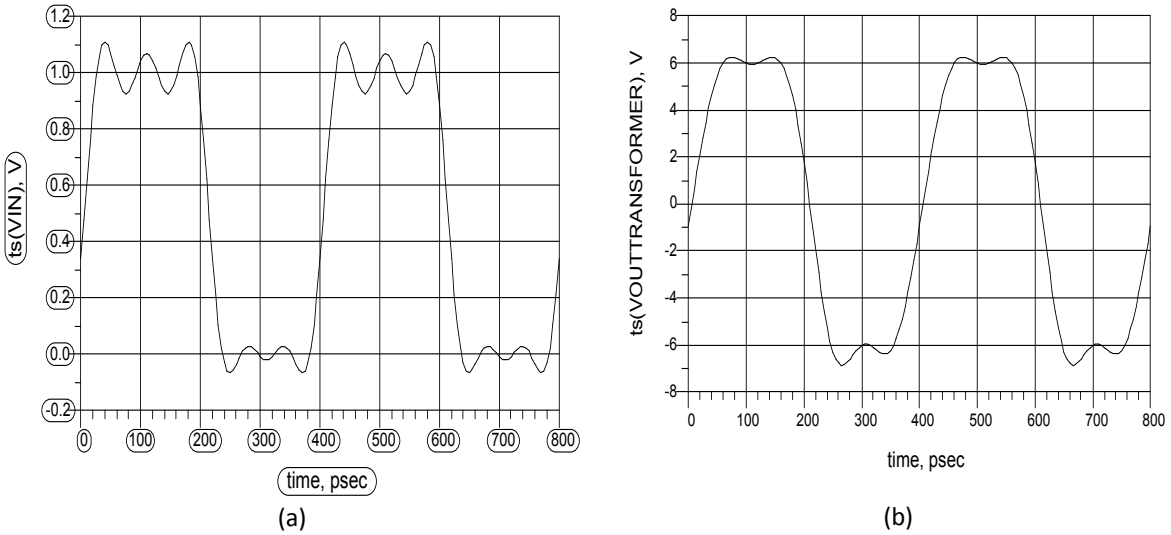

FIGURE 9. (a): The Input Pulse In 2.4Ghz (b): The Wave Seen at The Input of The CMOS

The impedances seen are:

$$ZL(W) = 0.245\text{-}5.195 \times \mathrm{j}$$

$$ZL(3W) = 0.079\text{-}1.747 \times \mathrm{j}$$

The input pulse is one volt with frequency of 2.4 GHz. The wave seen at the input of the CMOS is amplified and the ripple is reduced considerably, shown in figure 9(b). The input pulse is one volt with frequency of 2.4 GHz. The wave seen at the input of the CMOS is amplified and the ripple is reduced considerably, shown in figure 9(b).

IV. THE PROPOSED PA

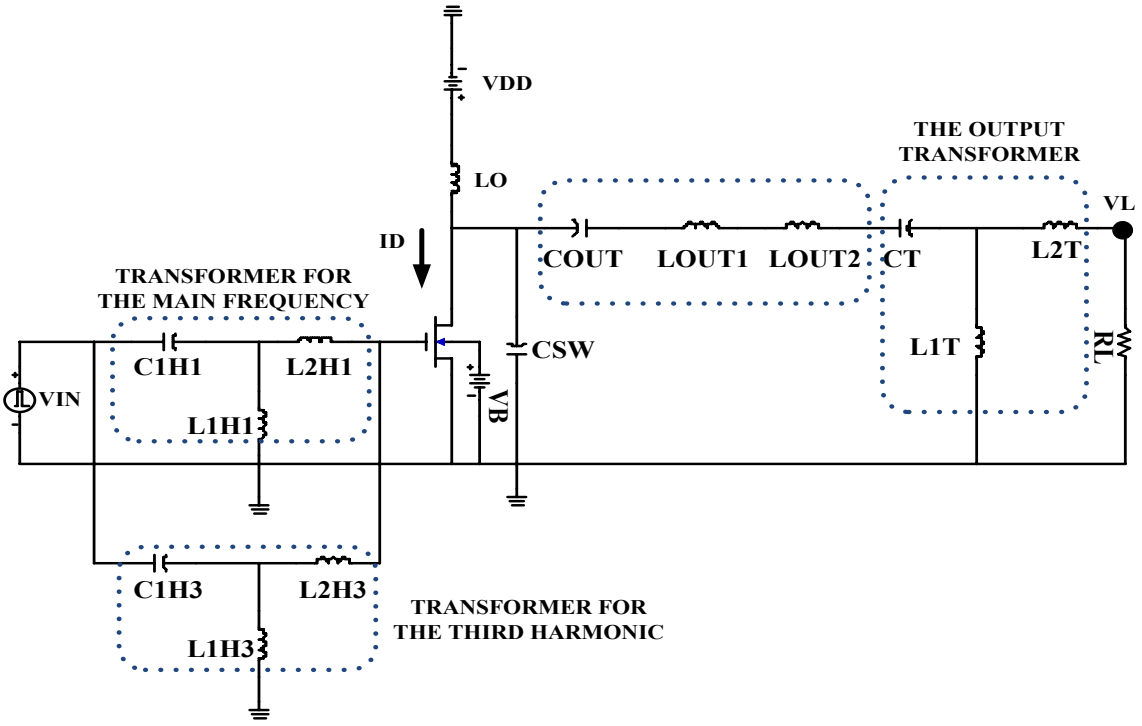

FIGURE 10. The Proposed power amplifier (PA)

The proposed circuit is comprised of:

1. An equivalent circuit of a transformer to amplify the input signal at the main frequency.
2. An equivalent circuit of a transformer to amplify the input signal at the third harmonic.
3. A CMOS acting as a switch.
4. A voltage supply (VB) connected to the BASE of the CMOS (forward body biasing technique).
5. Output elements to perform appropriately at the desired frequency in order to form a proper voltage for the output transformer.
6. The output transformer leading to the output load so as to amplify the signal applied to its input.

By connecting a voltage supply to the BASE of the CMOS or using the forward body biasing technique, the threshold voltage of the CMOS declines. As a result, the transistor is to produce bigger drain current with lower input voltage in the gate. In addition, the CMOS (the switch) can be turned on by lower input voltage, reducing power dissipation. Consequently, the lower input voltage is, the lower the power consumption of the input voltage supply (PIN) will be. Therefore, with lower PIN, higher PAE will be achieved. Plus, the bigger the drain current gets, the bigger output voltage will be, thus increasing the output power. Nevertheless, the bigger drain current might increase the power consumption of VDD. Although it might be debated that using another voltage supply can lead into more power dissipation, the power dissipated via VB is measured and it is approximately 1.38e-12 watts, which can be fundamentally ignored.

It is suggested that the output power of the class-E PA be calculated by equation (19) [10].

$$P_{OUT}=\frac{8}{\pi^2+4}\frac{V^2_{DD,PA}}{RL}\approx 0.577\frac{V^2_{DD,PA}}{RL} \quad (19)$$

The dependency of the Output power upon other parameters of the circuit is not mentioned in the equation (19). For instance, the role of elements belonging to the matching circuit, the drain current of the CMOS, the capacitor connecting to the drain of the CMOS, the inductor connecting to the drain of the CMOS, and the frequency at which the circuit is operating are not taken into account. Hence, the formula should cover all the parameters in order to clarify the relationship between the Output power and all parameters existing in the circuit. Thus, by taking ID as drain current, VL can be calculated by equation (20).

$$VL=\frac{ID\times RL}{\left(RL+L2T\times S\right)\times\left\{T1-\frac{\left(CSW\times S+\frac{1}{LO\times S}+T1\right)\times\left(\frac{1}{RL+L2T\times S}+\frac{1}{L1T\times S}+T1\right)\times\left(COUT+CT+COUT\times CT\times LOUT1\times S^2+COUT\times CT\times LOUT2\times S^2\right)}{COUT\times CT\times S}\right\}} \quad (20)$$

In which:

$$T1=\frac{COUT\times CT\times S}{COUT+CT+COUT\times CT\times LOUT1\times S^2+COUT\times CT\times LOUT2\times S^2} \quad (20a)$$

$$s=2\times\pi\times f\times j \quad (20b)$$

f : The frequency at which VL calculated.

$$j=\sqrt{-1} \quad (20c)$$

By considering ID as a complex number like $ID=\alpha+\beta\times j$, VL is rewritten in equation (21).

$$VL=\frac{\left(\alpha+\beta j\right)\times RL}{T2\times\left\{T1+\frac{\left(-\frac{j}{L1T\times\omega}+\frac{1}{T2}+T1\right)\times\left(-\frac{j}{LOUT\times\omega}+CSW\times\omega\times j+T1\right)\times\left(COUT\times j+CT\times j-COUT\times CT\times LOUT1\times j\times\omega^2-COUT\times CT\times LOUT2\times j\times\omega^2\right)}{COUT\times CT\times\omega}\right\}} \quad (21)$$

In which:

$$T1=\frac{COUT\times CT\times\omega\times j}{COUT+CT-COUT\times CT\times LOUT1\times\omega^2-COUT\times CT\times LOUT2\times\omega^2} \quad (21b)$$

$$\omega=2\times\pi\times f \quad (21a)$$

$$T2=RL+L2T\times\omega\times j \quad (21c)$$

Therefore, VL can be shown as equation (22).

$$VL = \frac{(rn + in \times j)}{(rd + id \times j)} \quad (22)$$

In which:

rn : The real part of the numerator.

in : The imaginary part of the numerator.

rd : The real part of the denominator.

id : The imaginary part of the denominator.

$$rn = \alpha \times COUT \times CT \times LO \times L4 \times RL \times \omega^2 \quad (22a)$$

$$in = \beta \times COUT \times CT \times LO \times L1T \times RL \times \omega^2 \quad (22b)$$

$$rd = (COUT \times L1T + COUT \times L2T + CT \times L1T + CT \times L2T) + (-CSW \times COUT \times LO \times L1T - CSW \times COUT \times LO \times L2T \times -CSW \times CT \times LO \times L1T - CSW \times CT \times LO \times L2T - COUT \times CT \times LO \times L1T - COUT \times CT \times LO \times L2T - COUT \times CT \times LOUT1 \times L1T - COUT \times CT \times LOUT1 \times L2T - COUT \times CT \times LOUT2 \times L1T - COUT \times CT \times LOUT2 \times L2T - COUT \times CT \times L1T \times L2T) \times w^2 + (CSW \times COUT \times CT \times LO \times LOUT1 \times L1T + CSW \times COUT \times CT \times LO \times LOUT1 \times L2T + CSW \times COUT \times CT \times LO \times LOUT2 \times L1T + CSW \times COUT \times CT \times LO \times LOUT2 \times L2T + CSW \times COUT \times CT \times LO \times L1T \times L2T) \times w^4 \quad (22c)$$

$$id = (CSW \times COUT \times LO \times RL - CT \times RL - COUT \times RL + CSW \times CT \times LO \times RL + COUT \times CT \times LO \times RL + COUT \times CT \times LOUT1 \times RL + COUT \times CT \times LOUT2 \times RL + COUT \times CT \times L1T \times RL) \times w + (-CSW \times COUT \times CT \times LO \times LOUT1 \times RL - CSW \times COUT \times CT \times LO \times LOUT2 \times RL - CSW \times COUT \times CT \times LO \times L1T \times RL) \times w^3 \quad (22d)$$

To separate the imaginary part from the real part of VL, equation (23) is utilized.

$$VL = \frac{(rn \times rd) + (in \times id)}{(rd^2 + id^2)} + \frac{(rd \times in) - (rn \times id)}{(rd^2 + id^2)} \times j \quad (23)$$

Once VL is calculated, the output power (pout) can be calculated from equation (24) and equation (25).

$$pout = \frac{VL \times conj(\frac{VL}{RL})}{2} \quad (24)$$

$$pout = \frac{NUMpout}{DENpout} \quad (25)$$

In which:

$NUMpout$: The numerator of the output power.

$DENpout$: The denominator of the output power.

$$NUMpout = (-RL \times \alpha^2 \times COUT^2 \times CT^2 \times LO^2 \times L1T^2 - RL \times \beta^2 \times COUT^2 \times CT^2 \times LO^2 \times L1T^2) \times w^6 \quad (25a)$$

$$DENpout = -2 \times (CSW \times COUT \times LO \times RL \times w^2 - CT \times RL - COUT \times RL + CSW \times CT \times LO \times RL \times w^2 + COUT \times CT \times LO \times RL \times w^2 + COUT \times CT \times LOUT1 \times RL \times w^2 + COUT \times CT \times LOUT2 \times RL \times w^2 + COUT \times CT \times L1T \times RL \times w^2 - CSW \times COUT \times CT \times LO \times LOUT1 \times RL \times w^4 - CSW \times COUT \times CT \times LO \times LOUT2 \times RL \times w^4 - CSW \times COUT \times CT \times LO \times L1T \times RL \times w^4)^2 - 2 \times (CSW \times COUT \times LO \times L1T \times w^3 - COUT \times L2T \times w - CT \times L1T \times w - CT \times L2T \times w - COUT \times L1T \times w + CSW \times COUT \times LO \times L2T \times w^3 + CSW \times CT \times LO \times L1T \times w^3 + CSW \times CT \times LO \times L2T \times w^3 + COUT \times CT \times LO \times L1T \times w^3 + COUT \times CT \times LO \times L2T \times w^3 + COUT \times CT \times LOUT1 \times L1T \times w^3 + COUT \times CT \times LOUT1 \times L2T \times w^3 + COUT \times CT \times LOUT2 \times L1T \times w^3 + COUT \times CT \times LOUT2 \times L2T \times w^3 + COUT \times CT \times L1T \times L2T \times w^3 - CSW \times COUT \times CT \times LO \times LOUT1 \times L1T \times w^5 - CSW \times COUT \times CT \times LO \times LOUT1 \times L2T \times w^5 - CSW \times COUT \times CT \times LO \times LOUT2 \times L1T \times w^5 - CSW \times COUT \times CT \times LO \times LOUT2 \times L2T \times w^5 - CSW \times COUT \times CT \times LO \times L1T \times L2T \times w^5)^2 \quad (25b)$$

V. RESULTS AND DISCUSSION

The output voltage and the shape of the output voltage is an important criterion. The output voltage in the fifth order of the harmonic balance analysis is formed by six waves including:

1- : The Direct Current (DC) voltage or the wave produced at f (frequency) =0 Hz.
2- VL (F1): The wave produced at the main frequency.
3- VL (F2): The wave at the second harmonic.
4- VL (F3): The wave at the third harmonic.
5- VL (F4): The wave at the forth harmonic.
6- VL (F5): The wave at the fifth harmonic.

$$VL(f1) = RVLf1 + IMVLf1 \times j \quad (26a)$$

$$VL(f2) = RVLf2 + IMVLf2 \times j \quad (26b)$$

$$VL(f3) = RVLf3 + IMVLf3 \times j \quad (26c)$$

$$VL(f4) = RVLf4 + IMVLf4 \times j \quad (26d)$$

$$VL(f5) = RVLf5 + IMVLf5 \times j \quad (26e)$$

In which:

$f1$: The main frequency.

$$f2 = 2 \times f1 \quad (26f)$$

$$f3 = 3 \times f1 \quad (26g)$$

$$f4 = 4 \times f1 \quad (26h)$$

$$f5 = 5 \times f1 \quad (26i)$$

$RVLfn$: Real part of the VL at nth harmonic.

$IMVLfn$: Imaginary part of the VL at nth harmonic.

Hence, the output voltage in the time domain can be calculated from equation (27).

$$\begin{aligned} VL_{tot}(t) = dc &+ \sqrt{IMVLf1^2 + RVLf1^2} \times cos(2 \times \pi \times f1 \times t + \tan^{-1}(\frac{IMVLf1}{RVLf1})) \\ &+ \sqrt{IMVLf2^2 + RVLf2^2} \times cos(2 \times \pi \times f2 \times t + \tan^{-1}(\frac{IMVLf2}{RVLf2})) \\ &+ \sqrt{IMVLf3^2 + RVLf3^2} \times cos(2 \times \pi \times f3 \times t + \tan^{-1}(\frac{IMVLf3}{RVLf3})) \\ &+ \sqrt{IMVLf4^2 + RVLf4^2} \times cos(2 \times \pi \times f4 \times t + \tan^{-1}(\frac{IMVLf4}{RVLf4})) \\ &+ \sqrt{IMVLf5^2 + RVLf5^2} \times cos(2 \times \pi \times f5 \times t + \tan^{-1}(\frac{IMVLf5}{RVLf5})) \end{aligned} \quad (27)$$

In which:

$\tan^{-1}$: The Inverse Tangent

The output voltage in time domain with different values of VDD and L1T is shown in figure 11. Indeed, with retaining all elements constant and altering just VDD and L1T, The PA can perform differently for different purposes. In fact, the trade-off between increasing the output power and decreasing the DC voltage (VDD) is compared in table1.

TABLE 1
The Trade-off between VDD and the Output Power

VDD(volt)	LIT(H)	Output Power(dBm)	PAE (%)
1	6e-9	18.58	69.049
1.18	5e-9	19.52	68.5
3.3	5e-9	28.5	68.36
3.4	4.33e-9	29.08	68.2
3.5	4.22e-9	29.28	67.13
3.6	4.47e-9	29.70	63.5
3.7	4.47e-9	29.93	63.3
3.8	4.36e-9	30.14	63.3
3.9	4.26e-9	30.3	63.3
4	4.15e-9	30.48	63.2
4.1	4.15e-9	29.28	63.2
4.2	4.46e-9	30.39	63
4.3	3.94e-9	30.48	62.8
4.4	4.30e-9	31.24	62.7

The PAs are supposed to fulfil two major objectives, including higher output power and higher PAE. Nonetheless, achieving both purposes might not be gained straightforwardly. Indeed, the output power is to increase provided that VDD is boosted. By raising VDD, power dissipation stemming from the DC voltage increases and PAE decreases. Hence, if the purpose is the high output power about 31.24 dBm, the more DC voltage is needed.

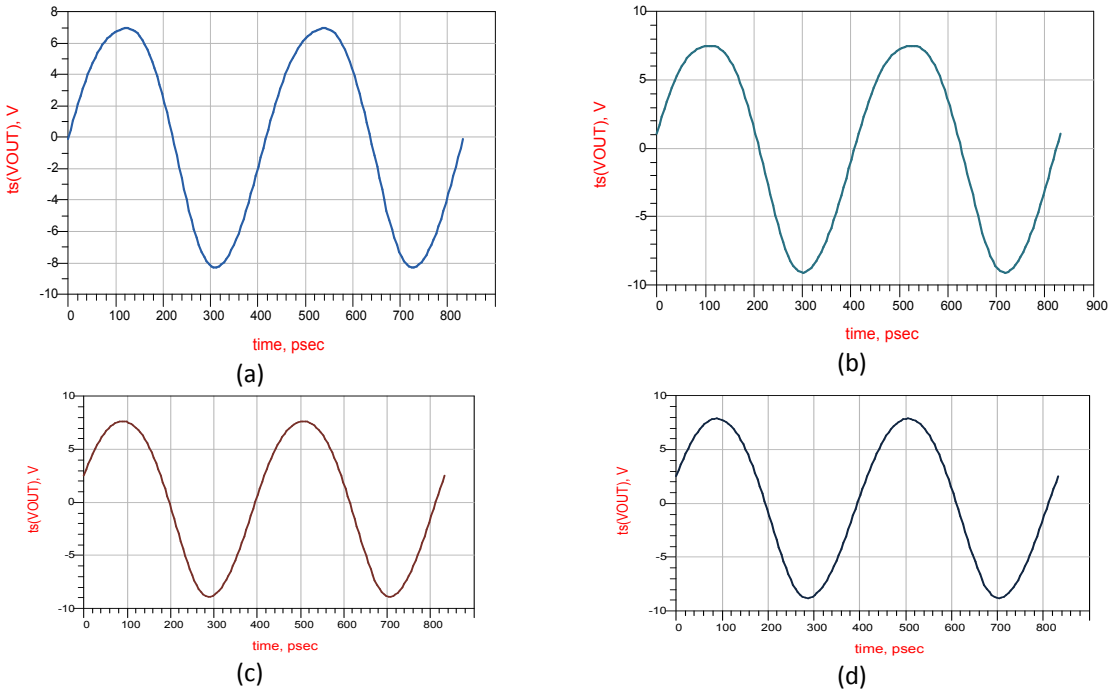

FIGURE 11. (a): VOUT with VDD=3.3 and LIT=5e-9 (b): VOUT with VDD=3.7 and LIT=4.47e-9 (c): VOUT with VDD=4 and LIT=4.15e-9 (d): VOUT with VDD=4.4 and LIT=4.30e-9

The output power and PAE of the PA are demonstrated in figure 12 and figure 13. The measured output power with VDD=1.18 and L1T=5 nH is about 19.52 dBm and PAE with VDD=1 and L1T=6 nH is about 69.049 percent. As expected, an appropriate output power is achieved with VDD=4.4 volts and the best PAE is gained with VDD=1 volt.

The performance of the proposed PA and other works at 2.4 GHz is compared in table 2. PAE is enhanced considerably by decreasing the input voltage technique via the utilization of two equivalent circuits of transformers. However, it is indisputable that an appropriate output power, about 28 dBm or 30 dBm, can not be gained without the higher VDD. The fact can be proven in both this work and other works by observing that the output power around 28 dBm or higher have been attained just with VDD=2.5 V or higher.

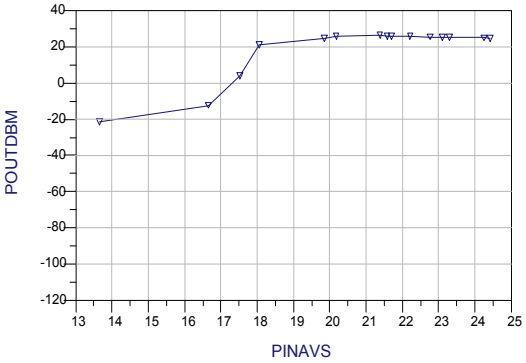

FIGURE 12. Output Power with VDD=1.18 and LIT=5e-9

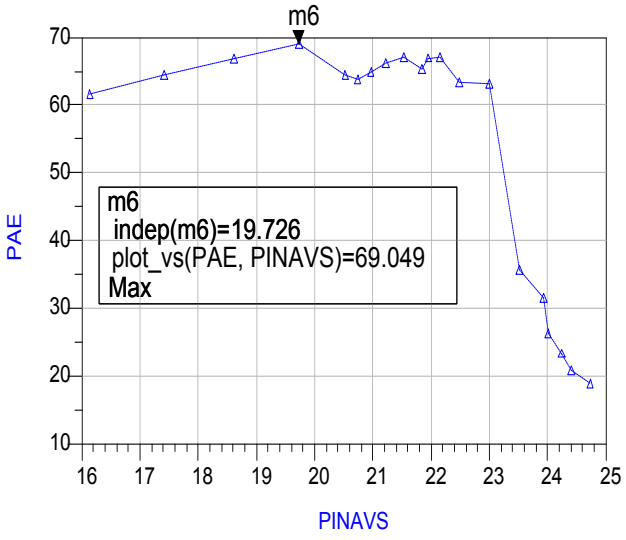

FIGURE 13. PAE with VDD=1, LIT=6E-9

Although the PAE is considerably increased, the value of the voltage supply is not appropriate. In fact, in order to achieve appropriate output power, the higher voltage supply is needed. Hence, the devices lifetime can be noticeably reduced. Plus, the power dissipation for both voltage supply and CMOS is increased. However, it is the trade-off between the desirable output power and the suitable PAE.

TABLE 2
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER STATE-OF-THE-ART AT F=2.4 GHz

Reference	CMOS Technology (µm)	Supply Voltage (V)	Classes	PAE (%)	Output Power (dBm)
THIS WORK	**0.13**	**1**	**E**	**69.049**	**18.58**
THIS WORK	**0.13**	**3.3**	**E**	**68.36**	**28.5**
THIS WORK	**0.13**	**4.4**	**E**	**62.7**	**31.24**
[1]	0.18	2.5	AB	31	26.8
[2]	0.18	2.4	F	34.6	27.6
[5]	0.18	1.8	D	50	15
[7]	0.18	2.4	-	49	24.5
[9]	0.18	1.6	E	35	18
[10]	0.13	2	E	57	19
[11]	0.13	2.5	-	44.7	20
[13]	0.18	3.3	A	34.3	25.2
[22]	0.18	3.3	E	44.5	23
[23]	0.18	3.3	E	40	21.3
[15]	0.35	1	E	33	18
[16]	0.18	3.3	-	34.9	23.3
[20]	0.18	3.3	AB	27	31
[24]	0.18	3.3	AB	29	30.7
[25]	0.13	2.5	AB	40	30
[26]	0.065	3.3	-	40.3	26.9
[27]	0.18	3.3	-	23.5	21.28

VI. CONCLUSIONS

A new design for a 2.4 GHz class E power amplifier is proposed in this paper. The notion of the performance of transformers is considered to increase PAE appropriately. Depending on the purpose of the circuit, the PA can be designed to have more output power with more VDD or decreasing VDD to reduce the power dissipation in the DC voltage supply. The proposed PA can perform properly with different VDDs just by modifying one element of the circuit. Although, the calculations of the output power and the output voltage is performed to simulate the circuit in 0.13 µm CMOS technology, the calculation is reliable for all other technologies. The calculations can justify the interdependency between the output power and all elements existing in the circuit. In this paper, the PA behaves differently with different voltage supplies. The best PAE, 69.049 %, is obtained with VDD=1 volt and the best output power, 31.24 dBm, is achieved with ADD=4.4 volt. Furthermore, the utilization of the equivalent circuit a transformer increases the PAE appropriately. Ultimately, the next step of this work can be continued to evaluate the proposed PA in smaller CMOS technologies. Plus, the circuit should be modified to perform in higher frequencies. In addition, the circuit can be enhanced to perform for the Ultra Wideband application.

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