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Hybrid Radix-4 SESA/SEDA Adders for Medical Image Processing

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ABSTRACT An adder is characterized as a digital circuit designed to compute the sum of numerical inputs, processing incoming binary digits and outputting their aggregate as a binary number. Digital adders play a crucial role in error-tolerant applications such as machine learning and image processing. However, a significant amount of power is typically consumed by traditional adders, posing challenges for energy-efficient circuit designs. This research is aimed at the development of adders that minimize power consumption without compromising performance, particularly for VLSI chips utilized in error-tolerant applications. A novel integration of hybrid radix-4 adders with Single Exact and Single Approximation (SESA) and Single Exact and Dual Approximation (SEDA) techniques is proposed that is both power-efficient and effective. Comprehensive simulations were conducted using the Xilinx ISE software, demonstrating that our SESA-RDx adders outperform conventional adders by achieving a power usage reduction of up to 58% and enhancing performance speed by up to 26.4%. The proposed hybrid adders signify a significant advancement in low-power adder design, providing a scalable and cost-effective solution for modern digital systems requiring energy efficiency without sacrificing accuracy.

INDEX TERMS Approximate Adders, Hybrid radix-4, Image Processing, Power Efficient, Xilinx ISE.

I. INTRODUCTION

In today's world of electronic systems approximation computing plays a crucial role. It is a computing approach that focuses on findings for accurate solutions to problems instead of exact ones. This method has gained popularity across industries due to the increasing need for energy high performance computing solutions [1]. While approximation computing offers advantages in terms of saving resources and boosting efficiency it is important to consider the balance between accuracy and resource conservation. The decision to embrace approximation computing depends on the requirements of application and the acceptable margin of error in the results. Approximate circuits, also known as inexact or unreliable circuits and they are designed to provide results that fall within a range of error rather than being exact. These circuits find applications in fields where strict precision is not energy efficiency and cost savings are valued [2]. They are particularly useful in image and signal processors for tasks like image resizing, filtering, audio and speech processing well as audio compression where a slight compromise, in quality can be tolerated. These approximate circuits are widely used for hardware accelerators in machine learning and deep learning.

Graphic Processing Units (GPUs) find utility across domains including gaming and scientific simulations. Approximate circuits can be used in graphics rendering to enhance real time performance while maintaining quality within a range. The extent to which approximate circuits are utilized depends on the demands of the application and the permissible margin of error. In some cases, the trade-off between reduced energy consumption, increased speed, and acceptable error margins makes approximate circuits a compelling choice.

Adders are fundamental building blocks in digital electronics and computer systems and it is primarily used for performing arithmetic operations, especially addition [23]. Adders can be found in various applications throughout the field of computing and electronics. Adders are two types and they are accurate and approximation adders. Accurate adders may consume more power and energy compared to approximation adders, making them less suitable for energy-efficient circuits. Accurate adders are essential when precision is critical, while approximation adders offer advantages in terms of speed, resource efficiency and energy savings [1]. Approximation adders are a type of digital adder circuit designed to perform addition operations with some degree of approximation. The primary concern of

approximation adders is minimizing power consumption, reducing hardware complexity and improving speed. Approximation adders are particularly useful in applications where a small loss in precision is acceptable or even imperceptible, such as multimedia processing, real-time signal processing, or low-power devices like IoT sensors. However, their use should be carefully considered based on the specific requirements of the application [2].

In digital circuits and representations, 'radix' refers to the base of a number system, which plays a crucial role in fields such as digital signal processing and data encoding. In the proposed system, hybrid radix 4 adders are integrated with SESA and SEDA adders for obtaining better simulation results. A hybrid radix-4 adder is a type of digital adder circuit that combines the principles of both radix-4 and non-radix-4 adders to optimize addition operations. Radix-4, radix-8 or other bases that are depends upon the specific application requirements. The goal is to achieve a balance between speed and hardware complexity by exploiting the advantages of different radix approaches.

Mostly in single approximation adders, the Least Significant Bit (LSB) is taken for approximate and Most Significant Bit (MSB) is considered as accurate. But in this proposed scheme, LSB is considered for SESA and SEDA approximation. On the other hand, MSB is maintained with hybrid radix 4 circuit. Radix 4 adder uses parallel computation approach [14]. This may lead to low power energy consumption and reduced delay when compared to other approximate adder circuits. The real time applications are implemented through MATLAB software.

In background work, the previous schemes and works related to hybrid approximation adders are analysed and discussed. Most of the previous works consists of different types of adders and they are described in this section.

Seyed et al., in [3] implements a memristor based approximate full adders. This scheme mainly works on the logic of imply methods. The energy consumption is about 68%. Though this system has numerous applications like image addition, image filtering. It lags in providing minimum error rate and commercial availability of memristor is low when compared to other transistors. To overcome this, Ayoub et al., in [4] describes about approximation adders and it follows approach that based upon nanotechnology. The delay of this scheme is given as delay of 2.16 ns and it provides average amount of power consumption when compared to other schemes. This approach gives binary image application. Chandan et al., in [5] describes a combination of imply logic and magic nor approximate adders. In this scheme, kodak datasets are used. Testbench results are simulated with pareto optimal designs and compared with other schemes. This scheme gives better bench mark results but does not mention power consumption and delay clearly. The results of digital image processing are not mentioned in detailed structures.

Gulafshan et al., in [6] presented MTJ hybrid approximate adders. The main target of this scheme is to reduce sensing energy and reduce area size. The proposed work is simulated with the help of HSPICE but does not clearly mention about image processing applications. MTJ uses mechanism known as spintronics and contain ferromagnetic properties. MTJ has numerous applications but this type of adder is costlier when compared to other approximate adders. Jungwon et al., in [7] implements a ERCPAA adder with the mechanism of prediction and truncation methods. Lena image is taken and demonstrated for image processing applications. In comparison with other approximation adders, ERCPAA has average power consumption delay. Other than digital image processing applications, this scheme is used for Neuromorphic computing and machine learning applications.

In order to rectify these approximate full adders disadvantages, Tanfer et al., in [8] proposed a LCA adder with LSB is approximated and MSB kept exactly. Monte carlo simulations were extracted in this scheme. This scheme has better RTL schematic design but lags in providing details about approximation adders real time application and analysis. Waqar et al., in [9] demonstrated LEADx adder for reducing error and it can implement in video processing applications. It has moderate PSNR value for various video sequences.

In [10] Kun et al., shows a hybrid radix 4 circuit for different VLSI applications. ACRA is a radix 4 adder and it works under both approximate and accurate modes. Though it has excellent image processing applications, it lags in providing important parameter low power consumption. Abdolah et al., in [11] describes a spintronic based adder for gaussian filter image processing applications and gives 47% improvements in power consumption. It reduces leakage current but cost of MTJ is not affordable and complex in market availability.

Padmanaban et al., in [12] shows a HOAANED approximate adder in Xilinx Artix-7. These HOAANED adder is experimented by various image dataset but power consumption, delay and other parameters are average when compared to few schemes. Weiqiang et al., in [13] designed an approximation adder for image processing applications. In this scheme they have approached majority logic technique, the circuit demonstrated here is said to be MLAFA and its NMED value is 0.083 [15]. The image processing applications is better when compared to other schemes but it does not provide power consumption and delay parameters [16].

From the existing schemes, overall interpretation of approximation adders is given in this section. Many schemes provide good image processing applications but lags in providing solutions for low power consumption and delay [17]. In most of the scheme's half of the bits are approximated and another half is left without any incorporation of mechanisms or techniques. Huge scheme approaches serial-based processing mechanisms [18]. To overcome these issues, our proposed system uses approximation technique along with fusion of radix 4 adder in MSB. Radix 4 adder works under the principle of parallel computing and reduces propagation delay and increase adder speed [19]. Proposed system uses single approximation techniques, it can work under both accurate and approximation modes.

The main objective of the proposed scheme is to design an efficient approximation adder with a focus on maintaining

low energy consumption. Additionally, the aim is to achieve better energy savings and minimize delay in operation. The organization of the remaining parts of our research article is as follows: Section II presents the proposed methodology, Section III elucidates the results obtained, Section IV delves into a comprehensive discussion, and the concluding section is our conclusion.

II. PROPOSED METHODOLOGY

A. HYBRID RADIX-4 MECHANISM

Radix-4 works under the principle of parallel computing i.e., proceeding two bits at same time. Due to this, hybrid radix 4 reduces propagation delay, improve power consumption of the system and increase processing speed [20]. Radix-4 consists of five inputs namely C_i, A, A_0, B, B_0 and three output is denoted as C_o, S_i, S_{i+1}. Here the input C_i is said to be carry input and A, A_0 denotes augend respectively. The parameter B, B_0 denotes addend respectively [21]. C_o, S_i, S_{i+1} is said to be carry output and sum of hybrid radix 4 respectively. The Boolean equation for hybrid radix 4 is formularized. Correctness proof (1), (2) and (3)

$$C_o = A_0B_0 + (AB)(A_0 + B_0) + C_i\big((AB)(A_0 + B_0)\big) \quad (1$$

$$S_i = (A \oplus B) \oplus C_i \quad (2)$$

$$S_{i+1} = (A_0 \oplus B_0) \oplus (AB + C_iA + C_iB) \quad (3)$$

The equation (1), (2), (3) denotes the outputs of radix-4 [14]. The Fast Fourier Transform (FFT) algorithm was developed to overcome the computational complexity. In FFT techniques, butterfly structures are used for computation and transforms [22].

B. SINGLE APPROXIMATION TECHNIQUES

Single approximation includes SESA and SEDA adders. Single approximation mechanism operates in accurate and approximate mode [23]. In SESA, single n bit accurate or approximate addition takes place but in SEDA the approach is quite different. SEDA can perform both single and dual n bit operations for accurate or approximate addition [24].

In SESA, the sum output is approximated and the carry left without approximation. Under single approximation SEDA, sum output is approximated and carry output will be depend upon the previous sum output and generate according to it [25]. Multiplexer is included in SEDA for conversion of sum into carry output. The single approximation technique has maximum bound error [26].The Boolean function of single approximation adders is given in the equations, correctness proof (4) and (5):

$$C_o = AB + BC + CA \quad (4)$$

$$S = \grave{C_o} \quad (5)$$

In equation (4) and (5), A, B *and* C are input of single approximation [14]. S denotes the sum and C_o denotes carry output.

C. INTEGRATION OF HYBRID RADIX-4 WITH APPROXIMATION TECHNIQUE (SESA-RDx and SEDA-RDx)

The given Fig. 1 shows the architecture of proposed system. The architecture consists of LSB, MSB parts and the single approximation takes place at LSB [27]. Additionally, at the MSB, exact hybrid radix-4 is exhibited. By using this mechanism propagation delay gets reduced and parameters for a signal processor will be satisfied as per the applications. n denotes the number of bits involved in single approximation mechanism [28]. Moreover, in single approximation mechanism PG signal is induced in input to determine whether the circuit works under accurate or approximate conditions [29].

When PG =1, bits in the sum and carry gets approximated and the circuit undergo approximate mode. Furthermore, when PG =0, under disable conditions circuit will operate in accurate state without any approximation. In inaccurate part, when PG gets enabled, sum gets approximated with

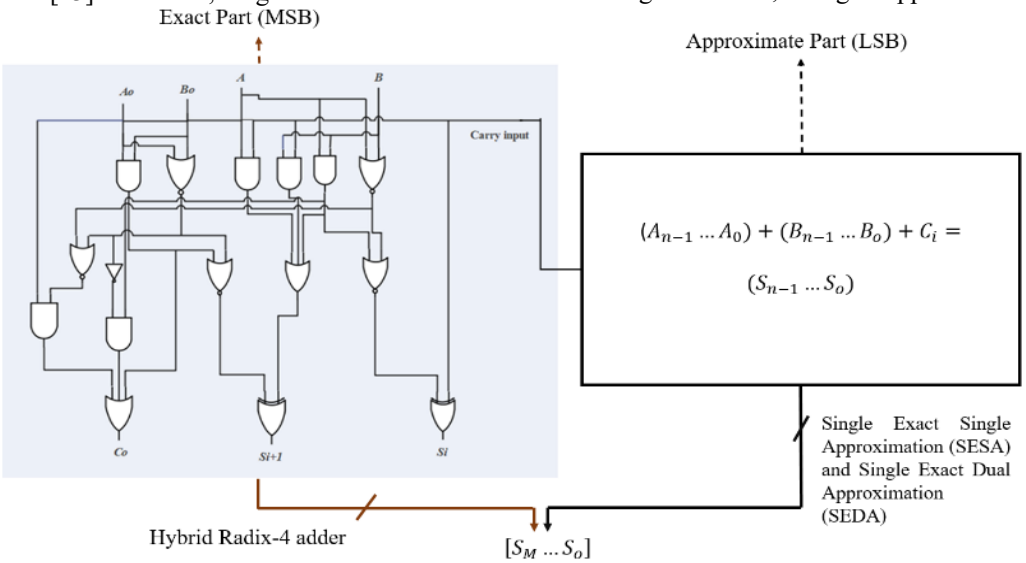

FIGURE 1. Architecture of hybrid radix-4 with single approximation mechanism Top of Form

the complement of carry [30]. Under exact part, approximate carry is given as input along with other inputs. In addition to that accurate i.e., exact part of the adder consists of hybrid radix-4 along with most significant bits are parallelly XOR-

ed and OR-ed at last for generating exact sum and carry. Single approximation mechanism exhibits under 8-bit,16-bit states [17]. For example, in 8- bit approximation takes place by approximating 0-3 bits in LSB and bit 4-7 bits in MSB are incorporated by hybrid radix-4 circuit. The output of the single approximation gets fetched and given as input to images in MATLAB software for developing real time applications [22]. Medical images are taken for analysing and diagnosis of several diseases such as brain tumour, neural disease and bone fractures etc., The focus of the proposed system is to give better results for enhanced medical images. The results of medical images are demonstrated and discussed in further sections.

III. RESULTS

Image smoothing is a method used to minimize the unwanted noise in an image by averaging the pixel values in the surrounding area of each pixel. On the other hand, image sharpening is a technique employed to improve the sharpness and intricacies of an image, giving it a more defined and clear appearance by increasing the high-frequency elements of the image. The size of the input image is taken as 256x256 and converted in to grayscale image for generating real time image processing applications. In this part, applications of proposed single approximation namely, image smoothening and image sharpening are simulated in MATLAB and its performance metrics are analyzed.

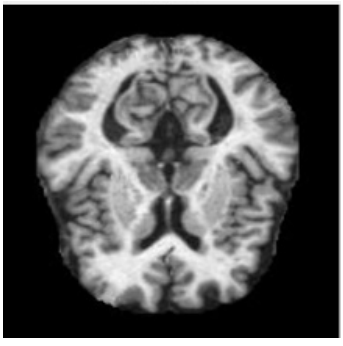

FIGURE 2. Image of Alzheimer Brain

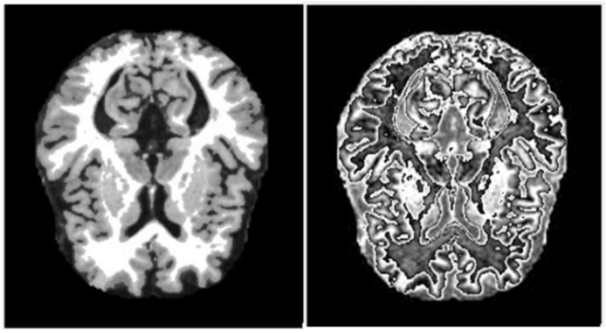

FIGURE 3. Image Smoothening and Sharpening of Existing SESA Adder

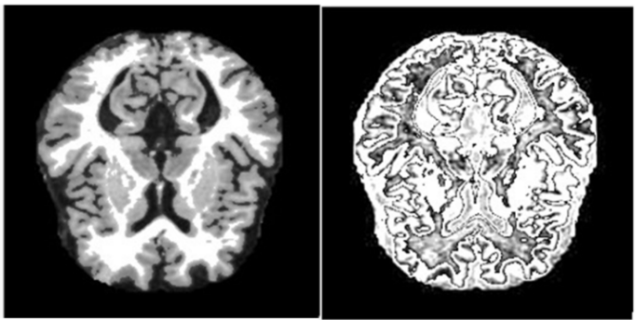

FIGURE 4. Image Smoothening and Sharpening Done By Existing SEDA Adder.

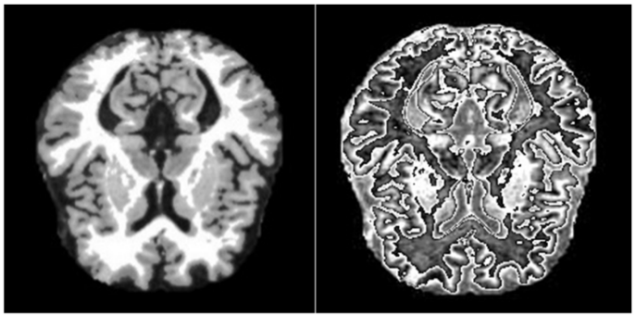

FIGURE 5. Image Smoothening and Sharpening by Proposed SESA-RDx Adder

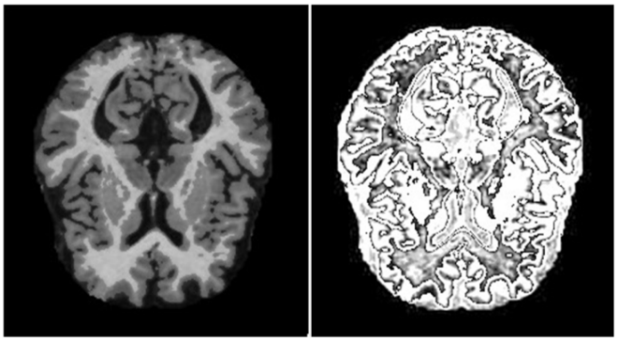

FIGURE 6. Image Smoothening and Sharpening by Proposed model of SEDA-RDx Adder.

Fig. 2 represents the brain activity image of patient affected by alzheimer disease. 16 bit of SESA- RDx and SEDA- RDx adders are given as input pixels for matlab image simulation. Furthermore, image soothening and sharpening are done for analysing the adder performance. Fig. 3 and 4 shows the applications of existing single approximation adders and Fig. 5, 6 represents applications of SESA-RDx, SEDA-RDx. PSNR stands for Peak Signal-to-Noise Ratio and SSIM stands for Structural Similarity Index Measure. Additionally, these metrics are commonly used to evaluate the quality of processed or reconstructed images in comparison to the original image. Moreover, PSNR and SSIM values are derived for the brain images. Table.1 describe PSNR and SSIM data for given image smoothen and sharpen of alzheimer brain images. Moreover, performance metrics and image simulated by SESA-RDx is well efficient when compared to SEDA-RDx.

TABLE 1
Metrics of single approximation adders

SINGLE APPROXIMATION ADDERS				
	Smoothening		Sharpening	
Methods	PSNR	SSIM	PSNR	SSIM
SESA-RDx (proposed)	24.321	0.921	21.061	0.895
SEDA-RDx (proposed)	19.358	0.902	18.795	0.827
SESA (Existing)	21.889	0.829	18.955	0.746
SEDA (Existing)	17.025	0.829	16.915	0.689

FIGURE 7, FIGURE 8, FIGURE 9, and FIGURE 10 show the graphical represntation of PSNR and SSIM of approximation adders applications. From the figure, it is described that highest PSNR and SSIM values are 24.321 and 0.921. Higher PSNR gives clear and accurate images as well as prediction of chronic disease will be easier.

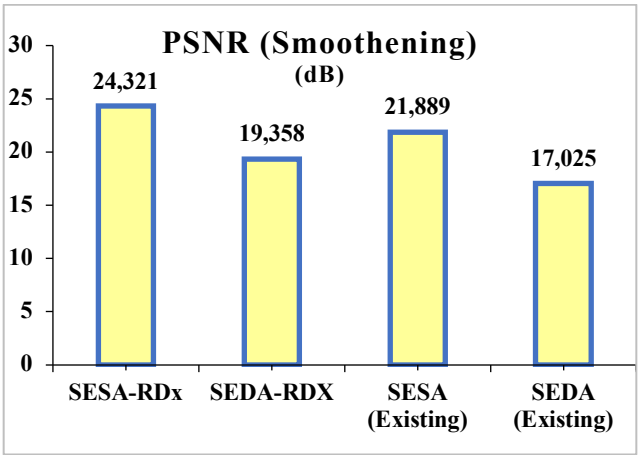

FIGURE 7. Comparison of Smoothening Metrics

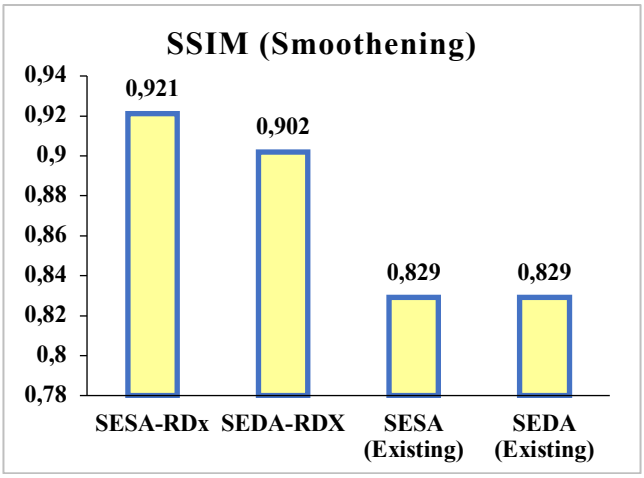

FIGURE 8. SSIM Smoothening Parameters of Single Approximation Adders

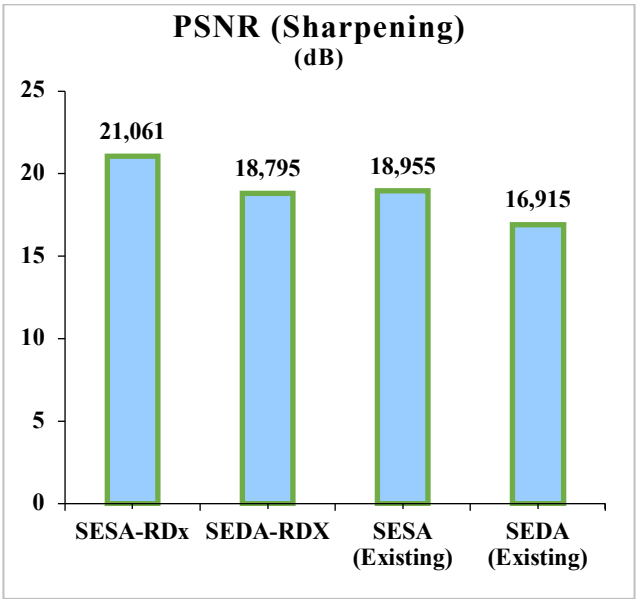

FIGURE 9. Image Sharpening Parameters

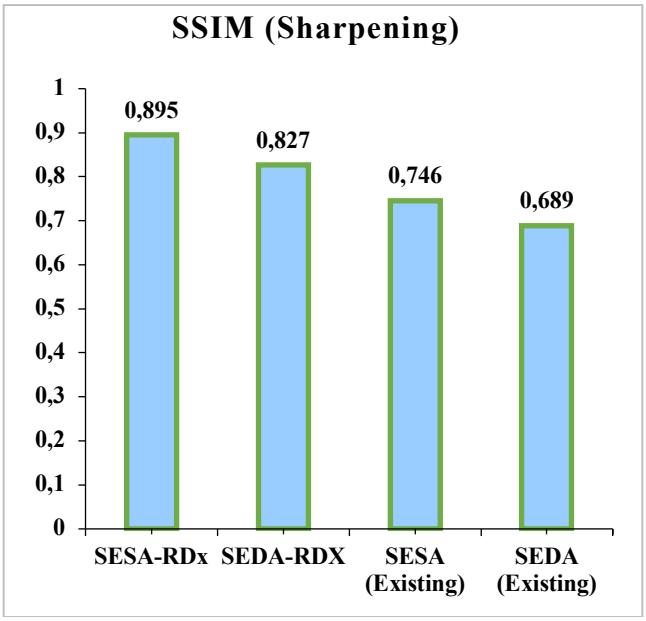

FIGURE 10. SSIM Parameters of Approximation Adders

IV.DISCUSSION

In Xilinx, Look-Up Tables (LUTs) serve as customizable memory blocks capable of executing logic functions, while Flip-Flops act as fundamental storage units holding individual bits of data. Gate delay represents the time required for logic gates to generate output signals upon receiving input signals, crucial for assessing operational speed. Power consumption is a pivotal consideration in system design, impacting energy efficiency and operational costs. Meanwhile, delay signifies the time taken for signals

to traverse different components within Xilinx, directly influencing system timing and overall performance.

TABLE 2
Comparison of approx. adders

Adder Design	LUT	FF	Gate Delay	Power (W)	Delay (ns)
APPROX 5	32	97	0.198	0.202	3.84
HEAA	28	88	0.190	0.201	3.19
HOAANED	30	90	0.189	0.192	2.95
SESA (Exist)	27	88	0.098	0.092	3.36
SEDA (Exist)	27	86	0.097	0.087	2.86
SESA-RDx (Proposed)	25	79	0.097	0.085	2.99
SEDA-RDx (Proposed)	24	73	0.095	0.083	2.83

In the realm of approximate adders, single approximation adders demonstrate superior efficiency compared to traditional counterparts due to the elimination of unnecessary transistor components and the utilization of pass transistors. Particularly noteworthy is the incorporation of the hybrid RD4 component at the Most Significant Bit (MSB), facilitating parallel computing and resulting in reduced resource utilization, power consumption, and delay. Moreover, this hybrid approach not only enhances computational efficiency but also fosters clearer input images and more accurate predictions, especially in applications such as chronic disease diagnosis.

The integration of hybrid approaches that combine various approximation techniques or dynamically select the most suitable technique for different function segments holds promise, particularly in medical imaging applications. By leveraging the strengths of different approximation methodologies, these hybrid approaches can enhance the efficiency and accuracy of medical imaging techniques, ultimately contributing to improved diagnostic capabilities and patient outcomes.

TABLE 1 compares different single approximation adders based on their performance in image processing tasks, specifically smoothing and sharpening. The proposed SESA-RDx adder outperforms others in both tasks, according to these metrics. Table 2 represents various adder designs such as APPROX 5, HEAA, HOAANED, SESA (Existing), SEDA (Existing), SESA-RDx (Proposed), and SEDA-RDx (Proposed), comparing and discussing their characteristics. TABLE 2 highlights the trade-offs between power consumption and delay across different adder designs. The proposed SEDA-RDx design stands out as the most efficient

FIGURE 11. Simulation of proposed SESA-RDx

FIGURE 12. Proposed SEDA- RDx simulated results

in terms of power while also offering competitive delay times, making it potentially valuable for applications where power efficiency is crucial. FIGURES 11 and FIGURE 12 depict the 16-bit SESA-RDx and SEDA-RDx simulations, while FIGURES 13 and FIGURE 14 provide graphical representations of power and delay for various approximate adders. It is observed in the figures that the power and delay of APPROX 5 are much greater than other approximate adders, while the proposed SEDA-RDx shows significantly lower values compared to various other adders.

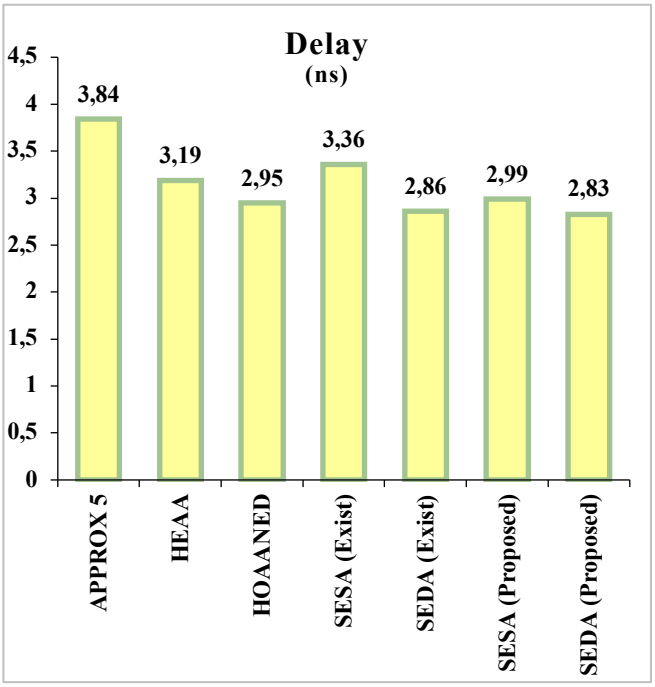

FIGURE 13. Power of approx. adders

TABLE 2 provides an in-depth analysis of various approximate adder designs, aiming to offer a comprehensive understanding of their performance characteristics and trade-offs. Our investigation encompasses a range of crucial metrics, including the utilization of Look-Up Tables (LUTs) and Flip-Flops (FFs), gate delay, power consumption, and overall delay. These metrics are pivotal in assessing the suitability of adder designs for different application scenarios.

Among the adder designs evaluated, the HOAANED design stood out with its remarkable achievement of the lowest gate delay, clocking in at just 2.95 nanoseconds. This swift processing capability makes it particularly well-suited for applications where rapid response times are imperative. On the other hand, the SEDA-RDx (Proposed) design showcased exceptional power efficiency, consuming a mere 0.083 Watts. Such low power consumption is crucial for energy-conscious applications, offering potential benefits in terms of reduced operational costs and extended battery life in portable devices.

Furthermore, our analysis revealed that the existing SEDA design exhibited the lowest overall delay, completing computations in just 2.86 nanoseconds. This finding underscores its efficacy in scenarios requiring high-speed processing, such as real-time signal processing or data streaming applications. However, it's important to note that each design presents its own set of advantages and limitations, necessitating careful consideration of the specific requirements and constraints of the target application.

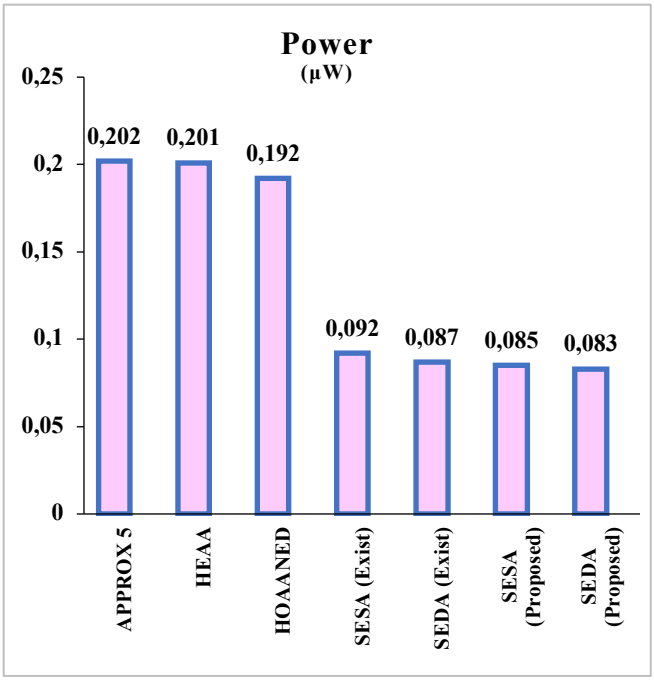

FIGURE 14. Delay of approx. adders

Xilinx simulation is conducted using tools such as the Design Suite to ensure the functionality and timing of hardware designs on Xilinx programmable logic devices. In the simulation, when the input signal is 1, the approximation of the adder takes place at 400 ns by approximating the first and last bit of the adder. This approach, while ensuring efficient approximation, inadvertently introduces a unique characteristic: when the adder operates in its accurate range, it triggers an error rate that subtly extends the processing time. This feature, initially appearing as a limitation, actually enhances the robustness of the scheme by dynamically adjusting the approximation precision based on the input signal, thereby contributing to a more adaptable and reliable system performance. Our study sheds light on the intricate interplay between performance metrics and design choices in the realm of approximate adder implementations. By providing insights into the relative strengths and weaknesses of different designs, we aim to empower designers to make informed decisions when selecting the most suitable adder architecture for their applications. Moving forward, further research endeavors could explore avenues for optimizing these designs to strike a more balanced compromise between speed, power efficiency, and resource utilization, thereby catering to a broader spectrum of application needs. Overall, our study contributes valuable insights to the ongoing

discourse on approximate adder design, facilitating advancements in FPGA-based system implementations.

V. CONCLUSION

This study successfully demonstrated the capabilities of single-approximation adders for improving medical image quality through smoothing and sharpening techniques. The evaluation of these adders reveals their potential for broad implementation across various technological domains, including microprocessor design. A critical analysis indicates that the APPROX 5 adder consumes 0.202 W of power, which is marginally higher than that of its counterparts. In contrast, the newly introduced SEDA-RDx demonstrates superior efficiency, with a power consumption of only 0.083 µW and a delay of 2.83 ns, outperforming other approximate adders in the field. The study further establishes that SESA-RDx outperforms SEDA-RDx in application performance metrics. Particularly in medical imaging, the deployment of SESA-RDx promises to significantly enhance image clarity, thereby improving the accuracy of chronic condition diagnoses. This research's ambition extends to the development of a MAC circuit with the aim of delving deeper into its practical applications.

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